[redacted]

UNITED STATES DISTRICT COURT
EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

NETLIST, INC., Plaintiff, v. SAMSUNG ELECTRONICS CO., LTD., et al., Defendants.	Civil No. 2:22-cv-00293-JRG **JURY TRIAL DEMANDED**

SAMSUNG'S 50(B) MOTION FOR JUDGMENT AS A MATTER OF LAW

[redacted]

TABLE OF CONTENTS

[redacted]

[redacted]

* All emphasis in this brief is added unless noted otherwise.

[redacted]

TABLE OF AUTHORITIES

Page(s)

Cases

Statutes

Other Authorities

[redacted]

[redacted]

TABLE OF EXHIBITS

#	Description
1	Excerpts from Defendants' Demonstratives
2	Excerpts from Plaintiff's Demonstratives
3	*Netlist Inc. v. Samsung Elecs. Co.*, No. 8:20-CV-00993-MCS-ADS, Dkt. 640 (C.D. Cal. Dec. 26, 2024)

TABLE OF ABBREVIATIONS

Abbreviation	Description
'215 patent	U.S. Patent No. 9,858,215
'417 patent	U.S. Patent No. 11,093,417
'608 patent	U.S. Patent No. 10,268,608
'912 patent	U.S. Patent No. 7,619,912
asserted patents	The '608, '912, and '417 patents
C.D. Cal.	U.S. District Court for the Central District of California
C.D. Cal. Case	*Netlist Inc. v. Samsung Elecs. Co.*, No. 8:20-CV-993 (C.D. Cal.)
DRAM	Dynamic Random Access Memory
DDR	Double-Data Rate
DIMM	Dual Inline Memory Module
JEDEC	Joint Electron Device Engineering Council
JDLA	Joint Development and License Agreement
JMOL	Judgment as a Matter of Law
LRDIMM	Load-Reduced Dual Inline Memory Module
MDQ	Module Data Input/Output
MDQS	Module Data Input/Output Strobe
MPR	Multi-Purpose Register
MRD	MDQS Read Delay Training
MWD	MDQ-MDQS Write Delay Training
Netlist	Netlist, Inc.
PDA	Per-DRAM addressability
RCD	Registered Clock Driver
RDIMM	Registered Dual Inline Memory Module
Samsung	Defendants Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., and Samsung Semiconductor, Inc.
SPD	Serial Presence Detect

[redacted]

INTRODUCTION

Defendants Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., and Samsung Semiconductor, Inc. move for judgment as a matter of law pursuant to Rule 50(b).

Final Judgment Is Premature. The Court prematurely entered final judgment in this case because Samsung's license defense remains a live issue. The Court specifically held that it would defer ruling on Samsung's license defense because "[w]hether or not such a license defense continues after such termination is controlled by and deferred to the Central District of California." Dkt. 768 at 3. The C.D. Cal. court has ordered a new trial on whether the JDLA has been terminated, wiping out the prior jury verdict in Netlist's favor. Dkt. 883-1 at 16. The Court should withdraw the Final Judgment until the C.D. Cal. Case has finally and fully resolved whether Samsung's license continues. Samsung is also filing herewith a motion to amend the judgment under Rule 59(e).

Noninfringement: Samsung is entitled to JMOL of noninfringement for each of the asserted patents—U.S. Patent Nos. 10,268,608, 7,619,912, and 11,093,417. Netlist did not present substantial evidence that the accused products meet the plain language of the claims. Indeed, Netlist's technical expert, Dr. Mangione-Smith, repeatedly ignored or contradicted the claim language, and his opinions thus do not support the verdict.

'608 Patent. All asserted claims require "buffer circuits" to delay a signal by an amount determined by a circuit ***within the data buffer*** of the accused products. Netlist failed to adduce substantial evidence that anything in the accused products' buffers "determines" a delay amount—the delay amount is instead determined outside of the accused products, ***in the host (memory) controller***. Netlist's expert conceded that the host controller's programming of buffer registers [redacted] Tr. at 534:24-535:3 (Mangione-Smith). Because the host controller determines the delay amount, and thus how the buffer operates,

[redacted]

Samsung is entitled to JMOL of noninfringement.

'912 Patent. Samsung is entitled to JMOL of noninfringement for three independent reasons. ***First***, Netlist's infringement case relied on the accused products' alleged capability to use two optional modes: (1) "PDA" mode, and (2) "Encoded QuadCS" mode. Even assuming that the modes satisfied the relevant claim limitations (which Netlist failed to show), Netlist also failed to show that the accused products are reasonably capable of using both modes together, as required to show infringement. ***Second***, the asserted claim requires transmitting a command signal to only one device at a time in response to "the set of input signals," including a "row/column address signal." Netlist's expert, however, contradicted the claim language by relying on "PDA mode," in which (a) the command signal is transmitted to ***multiple*** DRAMs (with as few as one DRAM executing the command and others ignoring it), and (b) row or column address signals cannot even be received. ***Third***, the asserted claim requires a memory module to have a "***first number of DDR memory devices*** arranged in a ***first number of ranks***" while receiving signals "configured to control a ***second number of DDR memory devices*** arranged in a ***second number of ranks***," where the ***second numbers*** are both ***smaller than the respective first numbers***.[1] But Netlist's expert opined that "Encoded QuadCS mode" satisfies this requirement solely based on the number of input signals—not the number of ranks or devices those signals are "configured to control." Notably, Samsung's products do not satisfy either the "second number of ranks" or "second number of DDR memory devices" limitations and thus Samsung is entitled to JMOL.

'417 Patent. All asserted claims require "data buffer control signals" (plural). Netlist

[1] The Court construed "rank" as "a 'bank' of one or more devices on a memory module that operate in response to a given signal." Dkt. 228 at 15, 35.

argued that a signal called "BCOM" satisfies the "data buffer control signals" term. Netlist's technical expert repeatedly testified that the BCOM signal is one signal, not multiple "control signals," as the claims require. Moreover, the claims specify that the "data buffer control signals" respond to a memory command to cause data transfer, but Netlist offered no evidence that Samsung's products use the BCOM signal in this manner. JMOL of noninfringement is therefore warranted.

Invalidity: Samsung is entitled to JMOL of invalidity as to the '608, '912, and '417 patents because the asserted claims lack written description support. A claim that has a broader scope than the invention described in its specification is invalid. Here, through continuation practice and overbroad, litigation-driven claim interpretations, Netlist stretched the asserted claims far beyond the alleged inventions disclosed in their specifications. No reasonable juror could have found otherwise.

No Willfulness: Samsung is entitled to JMOL that any infringement of the asserted patents was not willful. Netlist failed to offer sufficient evidence that, following Netlist's purported termination of Samsung's license to the asserted patents (which Samsung maintains was ineffective), Samsung engaged in any deliberate or intentional infringement.

BACKGROUND

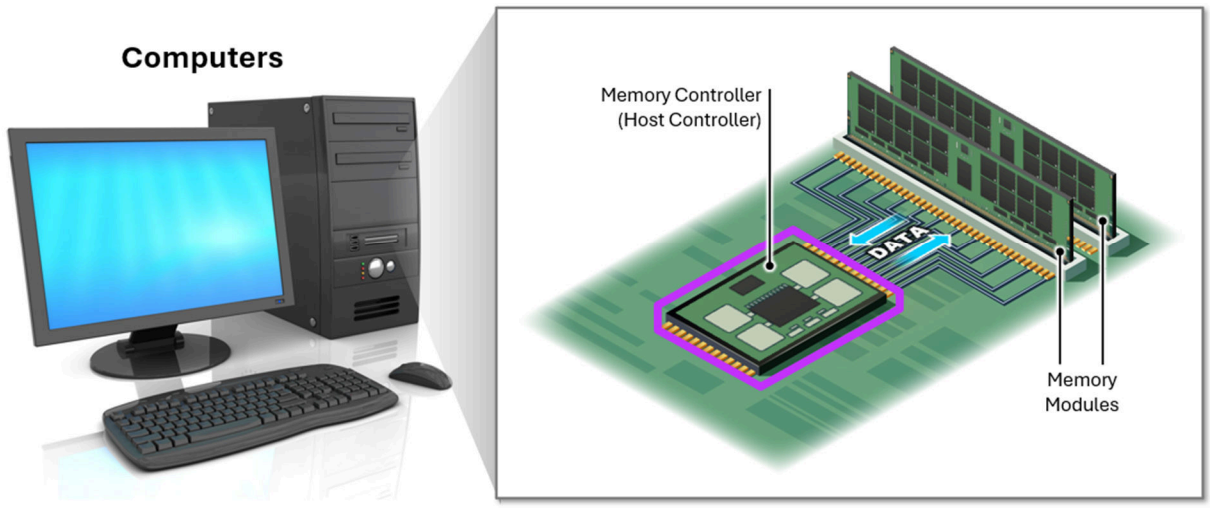
Netlist's third amended complaint in this action alleged infringement of four patents. Dkt. 100. After dropping one of those patents from the case (the '215 patent, Dkt. 325), Netlist proceeded to trial on the '608, '912, and '417 patents, asserting claims 1 and 5 of the '608 patent, claim 16 of the '912 patent, and claims 1, 2 and 8 of the '417 patent.

I. Background of Samsung and Accused Samsung Memory Modules

Samsung is a leading manufacturer of DRAM (Dynamic Random Access Memory) chips and sells memory modules incorporating those DRAM chips. Those memory modules fit into

[redacted]

slots on a computer motherboard and the computer's other components interface with the memory modules using a "memory controller," also called a "host" or "host controller." The memory controller can send various commands to the accused memory modules, such as "WRITE" or "READ," which respectively store or retrieve data.

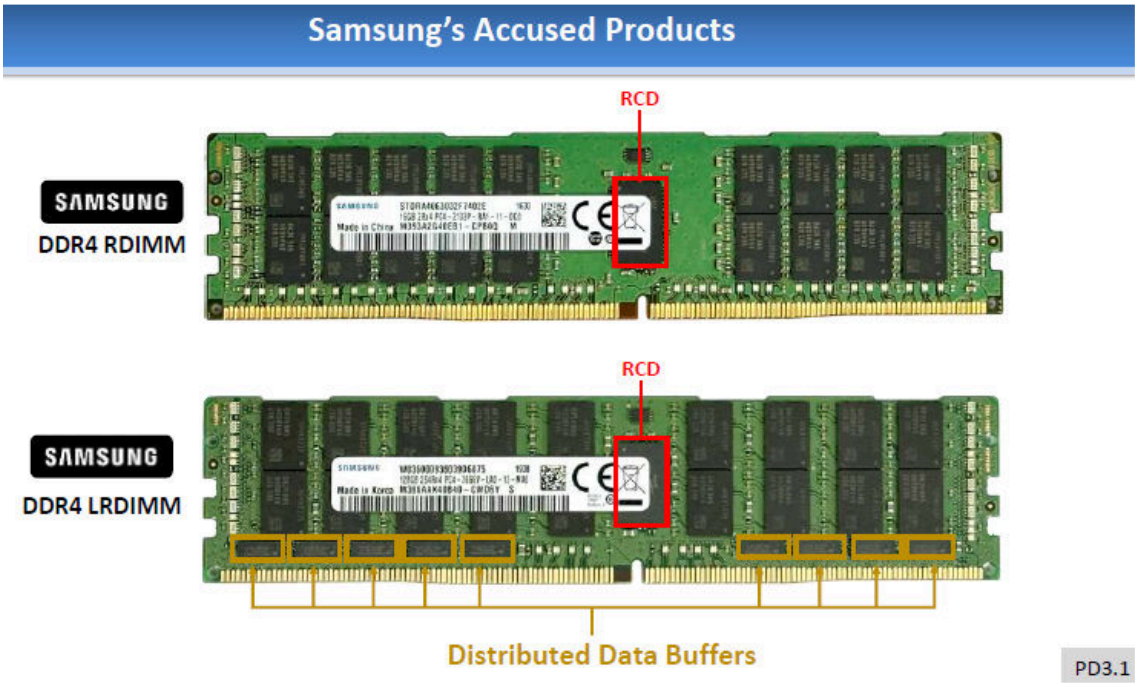


Ex. 1 at DDX4-1.

The accused memory modules are "dual" in-line memory modules (DIMMs) because they, unlike older, one-sided modules, have electrical contacts for transferring data on both sides. These memory modules are standardized products that comply with JEDEC DDR4 standards—the fourth generation of double-data rate (DDR) devices. These DIMMs arrange DRAM chips in groups known as "ranks," so that the group of chips may receive or store data together during the same memory command.

Two different kinds of Samsung DIMMs are at issue in this case—(1) Registered DIMMs (RDIMMs), and (2) Load-Reduced DIMMs (LRDIMMs). RDIMMs are accused of infringing only the '912 patent. LRDIMMs are accused of infringing all asserted patents. Both types of DIMMs have various components that JEDEC standards require, including DDR4 DRAMs,

serial presence detect devices (SPDs),[2] and registered clock drivers (RCDs).[3] LRDIMMs differ from RDIMMs in that they also include data buffers.[4] Samsung provides its own DDR4 DRAMs for its memory modules. Samsung sources other components, such as SPDs, RCDs, and data buffers, from third-party manufacturers like Montage, Renesas, and Rambus. One of Netlist's demonstratives, reproduced below, illustrates Samsung's RDIMM and LRDIMM products and the locations of the RCD and data buffer components in them:



Ex. 2 at PD3.1. The black, vertically-oriented rectangular chips in two rows are the DRAMs, with the RCD and Data Buffers as labeled. Tr. at 793:21-794:8, 795:2-5 (McAlexander).

[2] "[T]he SPD device, the serial presence detect device, . . . has the characteristics embedded in it of what the module is and it sends that exact information over to the controller." Tr. at 825:21-23 (McAlexander).

[3] The RCD "is the registered clock system, and this kind of orchestrates some of the timing on the circuit." Tr. 794:14-795:11 (McAlexander); *see also id.* 353:9-13 (Mangione-Smith) (explaining that RCD "stands for registered clock driver"). An RCD receives input signals from the host memory controller, such as chip select signals. *Id.* at 334:16-20 (Han).

[4] "[I]n the LRDIMM, the load-reduced DIMM, there are some buffer circuits in addition to the DRAMs that are used to interface to the computer." Tr. at 794:6-8 (McAlexander); *id.* at 409:20-23 (Mangione-Smith).

[redacted]

II. The Court Defers Judgment on Samsung's License Defense

As the Court has held, the JDLA granted Samsung a license to all the patents-in-suit. Dkt. 727. The Court thereafter clarified its summary judgment opinion: "The products in this case ***are*** covered by the license in the JDLA for as long as the JDLA remains effective" and "Samsung is entitled to a license defense ***at least*** up until Netlist's purported termination [of] the JDLA." Dkt. 768 at 2-3 (original emphases). Importantly, the Court reaffirmed its ruling that "[w]hether or not Samsung is entitled to a license defense ***after*** Netlist's purported termination depends on the outcome of the case in the Central District of California," which "controls the issues of termination and breach." *Id.* at 3 (original emphasis). The Court affirmatively declined to address Samsung's license defense and precluded Samsung from raising the defense at trial: "To be abundantly clear, Samsung has a license defense, in this case, at least up to July 15, 2020, when Netlist purported to terminate the JDLA. Whether or not such a license defense continues after such termination ***is controlled by and deferred to the Central District of California***." *Id.*

As of trial in this case, the C.D. Cal. court had not entered final judgment following the jury's verdict finding that Samsung breached the JDLA and post-trial motions in that case remained pending. Dkt. 768 at 2; Dkt. 727 at 1. On December 26, 2024, the C.D. Cal. court ordered a new trial and denied Netlist's motion for entry of judgment. Ex. 3 at 16. Accordingly, Samsung's license defense remains a live issue in this case and Samsung requests that the Court withdraw the Final Judgment here pending adjudication of the license issue in the C.D. Cal. Case.

III. Netlist Attempts To Prove Infringement by Ignoring the Claim Language

A. The '608 Patent

The '608 patent, titled "Memory Module with Timing-Controlled Data Paths in Distributed Data Buffers," describes a memory module comprising a "module control circuit,"

memory devices, and a plurality of "buffer circuits" coupled between memory devices located on the module and a host (memory) controller (such as a computer processor) located off the module. JX-3.2 (Abstract), .9 (Fig. 1), .36 (3:57-60). Each buffer circuit on the memory module includes a "command processing circuit" configured to decode signals from the module control circuit. JX-3.2 (Abstract), .34 (Fig. 19). Each buffer circuit also includes "a delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit," which is located within the buffer. JX-3.44 (cl. 1). Thus, both asserted claims of the '608 patent require that the buffer (specifically, the command processing circuit inside the buffer) determine the "delay amount."

At trial, Netlist asserted that Samsung's DDR4 LRDIMM products infringe claim 1 and claim 5, depending therefrom. Netlist's expert relied on a "training process" of the DDR4 LRDIMM products' buffers to allege that the buffer determines the delay amount, Tr. at 448:19-449:1 (Mangione-Smith), but he never explained how the training process works. His failure may be because the training process evidence plainly shows that the host (memory) controller determines the delay amount; the buffer merely implements the delay that the host (memory) controller has already determined and then programmed into the buffer. Netlist's expert testified that the buffers do things like storing, reading, and decoding the delay amount, contending that those actions amount to "determining" the delay amount. *See, e.g.*, Tr. at 446:19-24, 448:2-6, 448:12-14 (Mangione-Smith). However, Netlist failed to offer substantial evidence that the actions he identified are "determining" the delay amount under the plain meaning of this term. *Infra* Argument, § I.A.

B. The '912 Patent

The '912 patent, titled "Memory Module Decoder," describes a memory module that receives a set of input signals from a computer system (external to the memory module itself),

which signals are designed to control fewer memory devices and fewer ranks of memory devices than are on the memory module. JX-2.2 (Abstract). Specifically, asserted claim 16 requires the memory module to have a "first number of DDR memory devices arranged in a first number of ranks" and a "circuit" with a "logic element" "receiving a set of input signals . . . configured to control a second number of DDR memory devices arranged in a second number of ranks" where "the second number of DDR memory devices [is] smaller than the first number of DDR memory devices and the second number of ranks [is] less than the first number of ranks." JX-2.45 (cl. 16). Claim 16 further requires that those input signals include "at least one row/column address signal" and that the memory module's circuit "responds to . . . the set of input signals by . . . transmitting [a] command signal to only one DDR memory device at a time." *Id.*

At trial, Netlist asserted that Samsung's DDR4 LRDIMM and RDIMM products infringe claim 16 through their ability to support a combination of two different and very specific modes. First, to satisfy the requirement that "the command signal is transmitted to only one DDR memory device at a time," Netlist relied on per-DRAM addressability ("PDA") mode. Tr. at 403:4-407:1. Second, to satisfy the requirement of receiving a set of input signals "configured to control" fewer memory devices and ranks than are arranged on the module, Netlist relied on "Encoded QuadCS" mode. Tr. at 379:14-381:11. Both modes are optional and only the memory controller could modify the memory module to enter these modes. *Infra* Argument, § II.A.1. In view of the Court's holding that claim 16 is directed to "capability," Netlist needed to show that the accused products are "reasonably capable" of using both modes at the same time, but Netlist adduced no evidence on this issue.

Netlist's infringement theory also ignored the claim language. Netlist's expert testified that, in PDA mode, the memory module "allows programmability of a given device on a rank"

and thus causes a command signal to be "transmitted to only one DDR memory device at a time." Tr. at 403:11-404:17 (Mangione-Smith). But ***programming*** a single device is plainly not the same as transmitting a command to a single device, especially when PDA mode requires other devices to ***ignore*** the command ***transmitted*** to them. Nor did he explain how this command signal is sent in response to a "set of input signals" that comprises "at least one row/column address signal" as the claim requires. JX-2.45. This failure is unsurprising, as the unrebutted evidence shows that in PDA mode the memory module cannot receive row/column address signals ***at all***. Tr. at 836:19-840:9 (McAlexander); JX-30.29; JX-30.64. Netlist's expert further testified that, in Encoded QuadCS mode, the number of chip select inputs (one type of alleged input signal) received from a computer system is lower than the number of chip select output by a circuit on a memory module. Tr. at 380:10-381:11 (Mangione-Smith). The claim, however, require the input signals to be configured to control ***fewer memory devices and ranks*** than are on the memory module—the number of input signals is irrelevant.

C. The '417 Patent

The '417 patent, titled "Memory Module with Data Buffering," describes a memory module that uses a data buffer (described in the patent as a "circuit" or "circuitry" element) to control the flow of data between a memory bus and memory chips arranged in different ranks. JX-1.2 (Abstract). The memory module also includes a "logic" element that receives address, control, and chip-select signals for reading and writing data. *Id.* Independent claim 1 requires (1) the "logic" element to output "data buffer control signals" in response to a read or write memory command, and (2) the "circuitry" element to cause bursts of data transfers between the memory bus and memory chips in response to those "data buffer control signals." JX-1.59 (cl. 1).

At trial, Netlist asserted that Samsung's DDR4 LRDIMM products infringe independent

claim 1, and claims 2 and 8 depending therefrom. Netlist's expert testified that the DDR4 LRDIMM products' data buffers satisfy the claimed "circuitry" and the RCD component satisfies the claimed "logic." Tr. at 464:11-14, 473:14-19 (Mangione-Smith). In particular, he identified a particular signal transferred from the RCD to the data buffers, the "BCOM" signal, as the alleged "data buffer control signals." *Id.* at 469:8-11. Netlist did not offer evidence that the data buffers in the accused products cause bursts of data transfers between the memory bus and the memory chips in response to the BCOM signal as required by the claims. Instead, Netlist's evidence focused solely on whether the one BCOM signal was really multiple signals, despite the undisputed evidence plainly showing that the BCOM signal is a ***single***, four-bit signal. *Infra* Argument, § II.A.

D. Willfulness

The Court ruled that Samsung did not infringe (and thus did not willfully infringe) before Netlist's purported termination of Samsung's license to the asserted patents in July 2020. *See* Dkt. 727 at 27. Netlist argued that Samsung willfully infringed following the alleged license termination, but offered no evidence that Samsung took any actions, with respect to ***any*** asserted patent, after July 2020 or the filing of this action—other than continuing to sell the accused products, which is legally insufficient to demonstrate willfulness. Notably, Netlist's argument centered on vague documents from before the JDLA's alleged termination, none of which show that Samsung had reason to investigate Netlist's patents, let alone show that Samsung actually formed a belief that the patents were infringed. Nor could they, given the nature of Samsung and Netlist's interactions while Samsung was licensed and after the alleged termination of the JDLA.

IV. Samsung Moves for JMOL, the Jury Returns a Lump-Sum Verdict, and the Court Enters Final Judgment

At the close of evidence, Samsung moved for JMOL on several issues pursuant to Rule

50(a). Tr. at 1130:5-16. The Court granted Samsung's JMOL of noninfringement regarding any doctrine of equivalents theory, Tr. at 1176:4-6, but otherwise denied Samsung's motion for JMOL of noninfringement for each of the asserted patents, Tr. at 1175:25-1176:2. The Court also denied Samsung's motion for JMOL of invalidity for the asserted claims, Tr. at 1176:21-1177:3; and Samsung's motion for JMOL of no willful infringement, Tr. at 1177:4-5.

On November 22, 2024, the jury returned its verdict, finding that Samsung infringed at least one claim of each asserted patent. Dkt. 847 at 4. The jury found that the asserted claims of the '608, '912, and '417 patents are not invalid, *id.* at 5, and that Samsung's infringement was willful, *id.* at 6. The jury awarded $12 million for infringement of the '608 patent, $94 million for infringement of the '912 patent, and $12 million for infringement of the '417 patent. *Id.* at 7.

On December 2, 2024, the Court entered Final Judgment that: (1) Samsung infringed all asserted claims of the '608, '912, and '417 patents; (2) none of the asserted claims are invalid, and (3) Samsung willfully infringed the asserted claims. Dkt. 855 at 2-3. Despite the finding of willfulness, the Court determined that enhancement of damages pursuant to 35 U.S.C. § 284 was not appropriate. *Id.* at 2. The Final Judgment also awarded Netlist a lump-sum royalty and denied all "[a]ll other requests for relief now pending and requested by either Party but not specifically addressed herein[.]" *Id.* at 3. The Final Judgment fails to acknowledge the Court's previous ruling that it would defer ruling on Samsung's license defense. Dkt. 768 at 2-3.

APPLICABLE LEGAL STANDARDS

"When a case is tried to a jury, a motion for judgment as a matter of law is a challenge to the legal sufficiency of the evidence supporting the jury's verdict." *Cowart v. Erwin*, 837 F.3d 444, 450 (5th Cir. 2016) (internal quotation omitted). "JMOL should be granted when a party has been fully heard on an issue and there is no legally sufficient evidentiary basis for a reasonable jury to find for that party on that issue." *Montano v. Orange Cnty., Tex.*, 842 F.3d

865, 873 (5th Cir. 2016) (internal quotation omitted). The non-moving party must identify "substantial evidence" to support its positions. *TGIP, Inc. v. AT&T Corp.*, 527 F. Supp. 2d 561, 569 (E.D. Tex. 2007). "Substantial evidence is more than a mere scintilla. It means such relevant evidence as a reasonable mind might accept as adequate to support a conclusion." *Eli Lilly & Co. v. Aradigm Corp.*, 376 F.3d 1352, 1363 (Fed. Cir. 2004).

"Judgment as a matter of law of no literal infringement is appropriate if no reasonable fact finder could determine that the accused devices meet every limitation of the properly construed claims." *Elkay Mfg. Co. v. Ebco Mfg. Co.*, 192 F.3d 973, 980 (Fed. Cir. 1999) (reversing denial of judgment as a matter of law). A district court "correctly enter[s] judgment as a matter of law" of invalidity when "no reasonable jury could find the claims of the [asserted] patent meet the written description requirement." *Novozymes A/S v. DuPont Nutrition Biosciences APS*, 723 F.3d 1336, 1346 (Fed. Cir. 2013). To comply with this requirement, "[t]he written description must lead a person of ordinary skill in the art to understand that the inventors possessed the entire scope of the claimed invention." *Juno Therapeutics, Inc. v. Kite Pharma, Inc.*, 10 F. 4th 1330, 1337 (Fed. Cir. 2021); *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010).

"To establish willfulness, a patentee must show that the accused infringer had a specific intent to infringe at the time of the challenged conduct." *Provisur Techs., Inc. v. Weber, Inc.*, 119 F.4th 948, 955 (Fed. Cir. 2024) (quoting *BASF Plant Sci., LP v. Commonwealth Sci. and Indus. Rsch. Org.*, 28 F.4th 1247, 1274 (Fed. Cir. 2022)); *see also SRI Int'l, Inc. v Cisco Sys., Inc.*, 14 F.4th 1323, 1330 (Fed. Cir. 2021) ("[T]he concept of 'willfulness' requires a jury to find no more than deliberate or intentional infringement." (quotation, citation omitted)).

ARGUMENT

Based on the evidence presented at trial, Samsung is entitled to JMOL on the issues of

noninfringement, invalidity, and willfulness.

I. The Court Should Amend or Set Aside the Judgment as Samsung's License Defense Remains a Live Issue

The Court's Final Judgment, *inter alia*, denied all "[a]ll other requests for relief now pending and requested by either Party but not specifically addressed herein[.]" Dkt. 855 at 3. However, the Court previously held that it would defer ruling on Samsung's license defense:

> To be abundantly clear, Samsung has a license defense, in this case, at least up to July 15, 2020, when Netlist purported to terminate the JDLA. Whether or not such a license defense continues after such termination ***is controlled by and deferred to the Central District of California***.

Dkt. 768 at 3.

Samsung's license defense remains a live issue in this case because there is no final judgment in the C.D. Cal. Case. The C.D. Cal. verdict underpinning the applicability of Samsung license defense in this case has been set aside. Ex. 3 at 16. On December 26, 2024, the C.D. Cal. court ***ordered a new trial***, instructing the parties to file a joint statement by January 7, 2025, proposing dates for the new trial to begin no later than April 1, 2025. *Id.* Under these circumstances, the Final Judgment is premature and the Court should withdraw it until the C.D. Cal. Case has finally and fully resolved whether Samsung's license continues. *See* Fed. R. Civ. P. 60(a) ("The court may correct a clerical mistake or a mistake arising from oversight or omission whenever one is found in a judgment, order, or other part of the record."); *Rivera v. PNS Stores, Inc.*, 647 F.3d 188, 193-200 (5th Cir. 2011); *see also* Fed. R. Civ. P. 59(e).[5]

II. The Court Should Enter Judgment as a Matter of Law of Noninfringement and Invalidity of the '608 Patent

A. Samsung Is Entitled to JMOL of Noninfringement Because Substantial Evidence Does Not Support the Jury's Finding That the Accused Products' Data Buffers Determine the Delay Amount

[5] Samsung is also filing a motion to amend the judgment under Rule 59(e).

[redacted]

Substantial evidence does not support the jury's finding that the accused products satisfy the "determined" limitation of independent claim 1 of the '608 patent. The asserted claims require a memory module comprising, among other things, "a plurality of buffer circuits . . . each respective buffer circuit including . . . a command processing circuit . . . and a delay circuit ***configured to delay a signal through the data path by an amount determined by the command processing circuit***."[6] JX-3.44 (19:14-55). Netlist does not dispute that the command processing circuit in the claims doing the "determin[ing]" should be part of the data buffer on the memory module. Tr. at 570:1-5, 572:9-10 (Mangione-Smith). Netlist failed to adduce substantial evidence that the buffer in the accused products, as opposed to the host controller, satisfies this requirement.

1. The Host Memory Controller—Not the Data Buffer—Determines the Delay Amount

The parties presented evidence from the perspectives of the buffer and the host (memory) controller. In both instances, the jury heard a consistent message: the accused products use the memory controller to determine the delay, rather than the data buffer.

First, the evidence on the operation of the buffer demonstrates that it does not determine a delay, but instead receives the delay amount parameter from the memory controller. [redacted] Netlist's expert, Dr. Mangione-Smith, confirmed that the buffer depends on the host memory controller [redacted]

[6] Because the Court did not construe "determined," this term takes its plain and ordinary meaning. *See Broadcom Corp. v. Qualcomm Inc.*, 543 F.3d 683, 696 (Fed. Cir. 2008).

[redacted] *id.* at 529:5-8 (agreeing that the host "memory controller plays an essential role in programming the timing control registers [on the buffer]").

The testimony of Renesas engineer, Mr. Garret Davey—whom Dr. Mangione-Smith candidly admitted has spent more time studying the buffers at issue than he has, Tr. at 537:6-8 (Mangione-Smith)—likewise shows that the buffer does not determine the delay amount. [redacted].[7]

Second, the evidence on the host (memory) controller's operation confirms that the host (memory) controller, not the buffer, is responsible for determining the delay. The host (memory) controller training document from Intel, which makes the controller, states that [redacted]

[7] As discussed in Section I.A.2.b. below, Dr. Mangione-Smith offered only conclusory testimony regarding the source code.

[redacted] Samsung's expert, Mr. Joseph McAlexander, unequivocally testified that [redacted] Dr. Mangione-Smith even agreed with Mr. McAlexander that the host controller's programming of the buffer registers is what [redacted] Tr. at 534:24-535:3.

On this record, no reasonable jury could have concluded that the data buffers in the accused products determine the delay amount, as required by the claims.

2. The Record Lacks Substantial Evidence To Support the Judgment Based on Netlist's Infringement Theories

Unable to dispute the foregoing facts, Netlist offered two infringement theories at trial that disregard the claim language and its ordinary meaning. Netlist alleged that (1) buffer operations ***during*** the training process determine the delay time; and (2) buffer operations ***after*** the training process (and after the host programs the delay value into the buffer) also satisfy the claim language. Neither theory is supported by substantial evidence.

a. Netlist Failed To Offer Substantial Evidence That the Buffer Determines the Delay Amount *During* the Training Process

Netlist argued that the buffer determines the delay amount because "training occurs in the buffer" and the "data buffer uses a data pattern comparator to determine the exact language of the claim." JX-27.35; JX-32.50; Tr. at 1274:6-7 (Netlist closing) (arguing "Gatekeeping. JX-27 at 35. The training occurs in the buffer."); Tr. at 1274:7-9 (Netlist closing) (arguing "JX-27 at 35 [the data buffer datasheet] expressly says the data buffer uses a data pattern comparator to determine the exact language of the claim"); Ex. 2 at PD6.87.

First, under the plain meaning of the claims, it is not enough that training occurs in the buffer or that the delay amount is stored in the buffer. Rather, the claims require the buffer to ***determine*** a specific value—particularly, the buffer itself must determine the amount of delay.

[redacted]

JX-3.44 (19:14-55). Because Dr. Mangione-Smith flatly admitted that storing a delay is "a lot different" from determining a delay, Tr. at 528:22-24, the record unsurprisingly does not support Netlist's infringement theory.

Second, the statement Netlist argued allegedly shows the "data buffer uses a data pattern comparator to determine the exact language of the claim," Tr. at 1274:7-9, says nothing about determining a delay:

[redacted]

JX-27.35. Rather, this excerpt refers to one step that occurs during training—the matching step, as more fully described below. In the context of what happens during training mode, the buffer plainly does not "determine" the delay amount that should be used during normal operations by virtue of performing the matching step.

During training mode, the host determines the delay timing that the buffer will later use during normal operations. [redacted] For example,[8] the host (memory) controller writes the same data to registers on the buffer and to the DRAM, such as the pattern 0101. [redacted] Tr. at 808:9-15 (McAlexander). The host then causes the buffer to read the data from the DRAM for a range of delay values to identify

[8] Here, we provide an explanation of MRD training, which is used to determine the delay applied during read operations. For MWD training, the host follows a similar process as used in MRD training, but does so to determine the delay to apply during write operations. DTX-15.30-32; JX-27.35-36, .76-79, .96-99; JX-32.51-52, .85-88, .101-104.

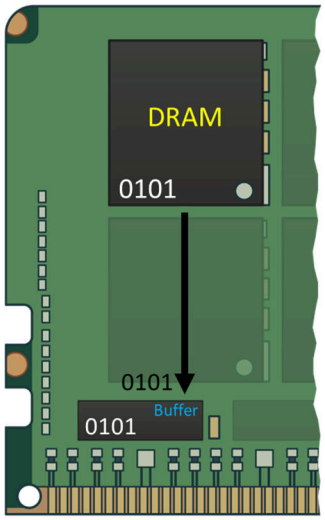
[redacted]

which of them cause the data to be read correctly. [redacted]

[redacted]

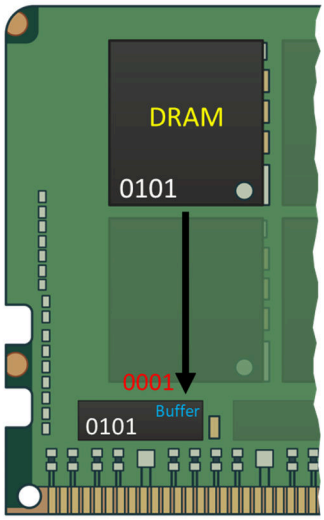
Specifically, for each delay value in the range, the buffer compares the data already in its registers to the data it reads from the DRAM. DTX-15.23; JX-27.33; JX-32.48; Tr. at 808:9-15 (McAlexander). For example, in the illustration in Figure 1a below, the data "0101" read by the buffer matches the data already stored in the buffer, also "0101," but in Figure 1b, the data "0001" read by the buffer does not match the data already stored in the buffer.

Fig. 1a



0101 = 0101
"Match"

Fig. 1b



0001 ≠ 0101
"No Match"

In the accused products, if the data already in a buffer's registers (set by the host) matches the data the buffer reads from DRAM, the buffer sends the host a "1"; if the data does not match, it sends the host a "0." DTX-15.23; JX-27.33, .35; JX-32.48, .50-51; Tr. at 807:22-808:24 (McAlexander).

The host, not the buffer, uses the information received during training mode to determine the delay. After receiving the "match" or "no match" signals for each value of tested delays, ***the host*** then determines which value in the delay range to instruct the buffer to use. [redacted]

[redacted] Intel, for example, [redacted] In other words, if the data matches for delay values of 1/64, 2/64, 3/64, 4/64, and 5/64, then the Intel controller [redacted] The host (memory) controller then programs the delay value it already determined into particular registers on the buffer, in the "buffer control words" block, so that the buffer will use this delay during normal memory operations. [redacted] JX-32.82, .84, .97-100; Tr. at 807:22-808:24 (McAlexander); [redacted]

Accordingly, although the host (memory) controller ***stores*** values in the buffer, including a range of delay values in training mode, the buffer is not the component that ***determines*** which delay value to use in operation. Rather, for each value in the range of delay values tested during training, the buffer simply informs the host whether there is a match between expected data and

[9] Netlist did not dispute Mr. McAlexander's explanation of the training process at trial. Dr. Mangione-Smith admitted that he did not look at the Intel training document or source code relating to the host (memory) controller. Tr. at 506:18-21 (admitting he "didn't look at a single product specification for any memory controller in this case"), 503:15-21 (same for source code).

[redacted]

data that is actually read or written. JX-27.35; JX-32.51. The host, not the buffer, determines which delay value the buffer will actually use in operation, and the host (memory) controller programs that delay value into the data buffer registers (by instructing the RCD to write the chosen delay value into the registers). [redacted]; Tr. at 529:5-8 (Mangione-Smith) ("The memory controller plays an essential role in programming the timing control registers. Yes? A. I would agree with that."). At no point does the buffer have any control over the delay value that the host (memory) controller programs into the data buffer's registers. Tr. at 805:10-23 (McAlexander).

Thus when Netlist's counsel argued in closing—without supporting expert testimony—that one step of the training, the matching step, satisfies the claim language, he was blatantly misrepresenting the evidence. Tr. at 1274:6-12 (Netlist closing). Instead of referring to the buffer's determining a delay value, [redacted] Tr. at 807:19-808:24 (McAlexander). The datasheet excerpt merely discusses the step in the training process where the buffer is determining whether the expected and actual data patterns ***match*** [redacted] as shown in Figures 1a and 1b above. JX-27.33, JX-27.35; JX-32.47-48, .50; Tr. at 808:9-19 (McAlexander). The excerpt says nothing about determining a delay amount, over which the buffer has no control. JX-27.35; JX-32.50; Tr. at 808:20-24 (McAlexander).

Notably, Dr. Mangione-Smith did not allege that the matching operation satisfies the claim language or even that the Renesas datasheet excerpt Netlist showed in closing had

anything to do with the buffer's determining ***a delay amount***. In fact, while he testified about the underlying document, Dr. Mangione-Smith ignored this portion of the datasheet. Tr. at 448:15-18, 449:9-11; JX-27.35. Netlist's unsupported attorney argument—the "data buffer uses a data pattern comparator to determine the exact language of the claim," Tr. at 1274:7-9 (closing)—is insufficient to support the jury verdict. *See Intell. Ventures I LLC v. Motorola Mobility LLC*, 870 F.3d 1320, 1331 (Fed. Cir. 2017) (holding "mere . . . attorney argument . . . [did] not provide substantial evidence supporting the jury's verdict of direct infringement"); *Correct Transmission, LLC v. Nokia of Am. Corp.*, No. 2:22-CV-343-JRG-RSP, 2024 WL 2026039, at *3 (E.D. Tex. Mar. 21, 2024) ("[A]ttorney argument is not evidence upon which the jury may rely."), *report and recommendation adopted*, 2024 WL 2428901 (E.D. Tex. May 22, 2024).

Accordingly, the record lacks substantial evidence that the buffer determines the delay value during training mode, as required to meet the claimed "command processing circuit." JX-3.44 (19:14-55) ("a delay circuit configured to delay a signal through the data path by ***an amount determined by the command processing circuit***").

b. Netlist Failed To Offer Substantial Evidence That the Buffer Determines the Delay *After* the Training Process Because Netlist Failed To Apply the Plain and Ordinary Meaning of "Determine"

Netlist ignored the claim language when it argued that operations the buffer executes after the training process qualify as the buffer's "determining" the delay value. Recall the claim requires "a plurality of buffer circuits . . . the each respective buffer circuit including . . . a command processing circuit . . . and a delay circuit configured to ***delay*** a signal through the data path by an ***amount determined by the command processing circuit***." JX-3.44 (19:14-55). The critical flaw in Netlist's theory is that it equates operations such as storing, reading, and decoding

[redacted]

the delay value with "determining" the delay value. The buffer's using a delay value that the host determined is not the same[10] as the buffer's "determining" the delay value. Tr. at 1253:9-13 (Samsung closing) ("When the Court tells us that we're going to take a 45-minute break for lunch, the Court has determined the delay. The Court has told us when we have to be back here. I may need to write it down so I don't forget, but I don't get to determine it.").

Netlist failed to offer substantial evidence that the actions Dr. Mangione-Smith identified—storing, reading, and decoding—are "determining" under the plain language of the limitation. Dr. Mangione-Smith provided no testimony on the plain meaning of "determining," let alone that it could mean storing, reading, or decoding values. Regarding "storing," Dr. Mangione-Smith admitted that "determining the amount of delay is a lot different from storing the amount of delay." Tr. at 528:22-24. Regarding "reading," reading a value from a stored location is plainly different from determining what that stored value should be so it can later be read. *Compare* JX-3.38 (7:41-42) ("reading from the SPD"), *with* JX-3.40 (12:33-34) ("determines a delay amount").

Regarding "decoding," the claim language belies any notion that one of ordinary skill thought decoding was synonymous with determining. The claims require that the command processing circuit "***decode*** the module control signals" but, in contrast, "***determine[]***" the "delay . . . amount." JX-3.44 (19:46-47, 19:52-54). [redacted]

[redacted]

[10] The Court granted Samsung's JMOL of noninfringement regarding any doctrine of equivalents theory. Tr. at 1176:4-6 ("I'm going to grant non-infringement as to the doctrine of equivalents so that it's prejudicial to being raised at a later time."). Therefore, the trial record must show that the action performed by the buffer is "determining" the delay amount, not just something arguably similar to "determining" the delay amount.

[redacted][11]

Dr. Mangione-Smith's attempt to recharacterize "determining" as storing, reading, or decoding is not substantial evidence of infringement under the plain meaning of the "determined" limitation. *See Exergen Corp. v. Wal-Mart Stores, Inc.*, 575 F.3d 1312, 1321 (Fed. Cir. 2009) ("No party may contradict the court's construction to a jury."); *Liquid Dynamics Corp. v. Vaughan Co.*, 449 F.3d 1209, 1224 n.2 (Fed. Cir. 2006) (holding "expert opinion evidence" was "irrelevant because it was based on an impermissible claim construction"). "[C]ourts can neither broaden nor narrow claims to give the patentee something different than what he has set forth." *Tex. Instruments Inc. v. U.S. Int'l Trade Comm'n*, 988 F.2d 1165, 1171 (Fed. Cir. 1993).

Finally, Netlist's conclusory testimony about the buffer source code does not provide substantial evidence that any buffer in the accused products determines an amount of delay.[12] Netlist argued in closing that the source code "taught you that those plusses and minuses mean that the calculation of the delay is in the buffer." Tr. at 1239:15-16. However, Dr. Mangione-Smith's testimony regarding the buffer source code and its supposed operation was conclusory and contradictory.

[11] [redacted]

[12] Dr. Mangione-Smith never provided a basis for a jury to conclude that the particular source code he examined was actually used in any accused product. There is no testimony from Renesas authenticating the source code or indicating that the particular code Dr. Mangione-Smith identified is actually found in any accused product.

[redacted]

For example, he alleged certain values in the code corresponded to the delay:

[redacted]

[redacted] Dr. Mangione-Smith then alleged certain separate source code for the buffer (i.e., code he asserted was for the buffer's transaction control circuitry) [redacted]

[redacted]

[redacted]. Elaborating further, Dr. Mangione-Smith alleged that the transaction control circuitry is multiplying and adding undisclosed information after "looking up the value stored" in the buffer registers (which he elsewhere called tables) by the host (memory) controller:

> [W]hat the transaction control circuitry is doing is it's looking up the value stored in these four registers and it's ***multiplying some of the information*** out of there and then ***adding it together with other information*** and then ***dividing it by another number*** and determining exactly how much delay should be done to each individual bit line, one bit line coming out of the data buffer for a write operation.

Tr. at 446:25-447:6.

However, Dr. Mangione-Smith never explained the operation of the source code in the detail necessary for his testimony to qualify as substantial evidence. Tr. at 451:7-454:17. The source code itself is not in evidence and thus cannot support the infringement verdict. Dr. Mangione-Smith did not explain what "information" or "numbers" are allegedly used to determine what he said is the delay amount. *Id*. He did not explain any step in the code that purportedly determines the delay, or explain the inputs to that step. *Id*. Accordingly, his opinion is too conclusory to support the verdict. *MobileMedia Ideas LLC v. Apple Inc.*, 780 F.3d 1159, 1172 (Fed. Cir. 2015) ("Conclusory statements by an expert . . . are insufficient to sustain a

[redacted]

jury's verdict.").

Although Dr. Mangione-Smith showed the jury two demonstratives, PD3.16 and PD3.17, those demonstratives are likewise not in evidence. Even if they were, they illustrate further that Dr. Mangione-Smith provided nothing more than *ipse dixit* opinions on the source code. [redacted] Given this mismatch, no reasonable jury could have relied on his testimony about the source code to find infringement. *Guile v. United States*, 422 F.3d 221, 227 (5th Cir. 2005) ("An expert's opinion must be supported to provide substantial evidence; 'we look to the basis of the expert's opinion, and not the bare opinion alone. A claim cannot stand or fall on the mere *ipse dixit* of a credentialed witness.'" (quoting *Archer v. Warren*, 118 S.W.3d 779, 782 (Tex. App. 7th 2003))); *Viterbo v. Dow Chem. Co.*, 826 F.2d 420, 422 (5th Cir. 1987) ("If an opinion is fundamentally unsupported, then it offers no expert assistance to the jury.").

Accordingly, Netlist lacks substantial evidence that the buffer determines the delay value, as required by the claims and the Court should enter JMOL of no infringement.

B. There Is No Evidentiary Basis To Conclude That the '608 Patent's Written Description Adequately Discloses Determining a Delay Amount

The Court should enter JMOL of invalidity for the '608 patent because the specification lacks written description support for the claims as Netlist applied them in this case. Here, the

claims require "delay[ing] a signal through the data path by an amount determined by the command processing circuit." Netlist does not dispute that the command processing circuit in the claims doing the "determin[ing]" is in the data buffer on the memory module. Tr. at 570:1-5, 572:9-10 (Mangione-Smith). Yet, Netlist read the claims on buffers that merely use a delay determined by a non-accused, off-module memory controller. Netlist's impermissibly broadening the claims in this way invalidates them. *Rivera v. Int'l Trade Comm'n*, 857 F.3d 1315, 1321 (Fed. Cir. 2017) (holding claims invalid, in part, because "even applying the 'broad' definition of 'pod' as 'a package formed of a water permeable material and containing an amount of ground coffee or other beverage therein,' written description support for broad claims covering a receptacle with integrated filter such as Solofill's accused products and Rivera's Eco-Fill products is lacking").

First, the '608 patent itself teaches away from using a memory controller, calling conventional systems that use a memory controller to ensure proper timing of the data signals "insufficient." JX-3.35 (2:28-36); Tr. at 799:4-15 (McAlexander). In particular, the '608 patent describes two approaches to addressing signal delays in memory modules: one using a memory controller to "insure [sic] proper timing" and the other (the claimed system) that uses the buffer to "determine" an amount of delay. JX-3.35 (2:28-36), .44 (cl. 1). The '608 patent itself distinguishes these two approaches and criticizes using the off-module memory controller to address the problem: "In some conventional memory systems, the memory controllers include leveling mechanisms . . . ***such leveling mechanisms are also insufficient to insure proper timing***[.]" JX-3.35 (2:28-36). Instead of using memory controllers to "[e]nsure proper timing," the '608 patent discloses using a buffer on the memory module to determine the delay. JX-3.2 (Abstract) ("The memory module comprises … a plurality of buffer circuits[.] . . . Each

respective buffer circuit includes . . . a command processing circuit . . . and a delay circuit configured to ***delay a signal through the data path by an amount determined by the command processing circuit*** . . . ."); Tr. at 799:24-800:11 (McAlexander).

Second, every embodiment in the patent teaches using the data buffer (also referred to as an "isolation device" or "ID")—and only the data buffer—to determine the timing of any delay. JX-3.40 (12:30-37), .42 (15:42-45, 16:10-12). At trial, however, Netlist advanced an interpretation of the claim broadening it to include what Netlist characterized as the buffer determining the delay amount with the assistance of another component (i.e., the memory controller). Tr. at 860:15-861:15 (McAlexander); Tr. at 528:25-529:3 (Mangione-Smith) (stating the memory controller is "involved in [programming the data buffer's timing control registers]. It does that in coordination with the RCD and the data buffer itself, sure"); *see also id.* at 529:5-8. But the written description never teaches the scenario where a buffer receives a delay value determined by the memory controller. It also does not disclose, teach, or even suggest an arrangement where any off-module component assists the on-module buffer in determining a delay amount. Every embodiment teaches that all one needs is circuitry within the buffer (or isolation device "ID") to determine the delay amount. JX-3.40 (12:30-37) ("[T]he ***ID control circuit 310*** further includes a delay control circuit 650 that . . . ***determines a delay amount*** to be used by the DQ routing circuit 320 and the strobe routing circuit 620.").[13]

Netlist thus uniformly informed the public that a buffer alone determines a delay amount. Netlist's later broadening the claim at trial to capture a different arrangement—that the patent

[13] *See also* JX-3.42 (15:42-45) ("The time interval between t4 and t3, referred to hereafter as an enable-to-write ***data delay EWD, can be determined by the isolation device 118*** since both these signals are received by the isolation device."); JX-3.42 (16:10-12) ("The time interval between t4 and t3, i.e., the enable to ***write data delay EWD, is determined by the delay control circuit 650 in the ID control circuit 310***, as shown in FIG. 6.").

[redacted]

itself disparages—renders the claim invalid. *See Atl. Rsch. Mktg. Sys., Inc. v. Troy*, 659 F.3d 1345, 1355 (Fed. Cir. 2011) (affirming summary judgment of invalidity because "claims 31-36 exceed in scope the subject matter that inventor Mr. Swan chose to disclose to the public in the written description").

Finally, the record is wholly one-sided on the lack of written description here because Netlist failed to present a rebuttal case against the '608 patent's invalidity. Mr. McAlexander testified that a skilled artisan would not have understood the named inventors to have had possession of an invention where the memory controller determines the delay amount. Tr. at 817:16-818:9; *see also* Ex. 1 at DDX4-3 ("The '608 patent claims are invalid: no disclosure of a system where the memory controller determines the amount of delay."). He also directly addressed Netlist's theory and explained that the patent does not support claims covering the memory controller's providing even a "contribution" to the process of determining the delay amount. Tr. at 817:16-22. Dr. Mangione-Smith never provided any testimony to the contrary; he could not even remember what the inventor said about what entity was supposed to determine the delay. Tr. at 537:22-538:7. Therefore, the record lacks any evidence showing the specification supports claims broad enough to cover off-module components determining the recited delay. *See ParkerVision, Inc. v. Qualcomm Inc.*, 621 F. App'x 1009, 1023 (Fed. Cir. 2015) (reversing "the district court's denial of Qualcomm's motion for JMOL of invalidity" because "there is no basis on which a reasonable jury could reject" the expert's "uncontradicted testimony").

Accordingly, the Court should enter JMOL of invalidity for the '608 patent.

III. The Court Should Enter Judgment as a Matter of Law of Noninfringement and Invalidity of the '912 Patent

A. Samsung Is Entitled to JMOL of Noninfringement of the '912 Patent

[redacted]

Netlist's infringement case for claim 16 relied on the accused products' alleged capability to use two optional modes. To satisfy the requirement that "the command signal is transmitted to only one DDR memory device at a time," Netlist relied on per-DRAM addressability ("PDA") mode. Tr. at 403:4-407:1 (Mangione-Smith). To satisfy the requirement of receiving a set of input signals "configured to control" fewer memory devices and ranks than are arranged on the module, Netlist relied on "Encoded QuadCS" mode. *E.g.*, Tr. at 379:14-381:11 (Mangione-Smith). This infringement read was deeply flawed.

First, even under the incorrect assumption that both PDA mode and Encoded QuadCS mode satisfy the relevant claim limitations, Netlist failed to show that the accused products are reasonably capable of using both modes together, as is required to show infringement. *E.g.*, *INVT SPE LLC v. Int'l Trade Comm'n*, 46 F.4th 1361, 1375-76 (Fed. Cir. 2022) ("Where claim language recites capability as opposed to actual operation, an apparatus that is reasonably capable of performing the claimed functions without significant alterations can infringe those claims." (quotation marks omitted)).

Second, PDA mode cannot transmit a command signal to only one memory device at a time; rather, it allows as few as one device to execute the command by informing other devices to "ignore" that command. Tr. at 406:1-8 (Mangione-Smith); JX-30.64. Moreover, claim 16 requires transmitting the command signal to only one device at a time in response to "the set of input signals," including a "row/column address signal," and commands in PDA mode are never sent in response to row or column address signals. JX-2.45.

Third, Encoded QuadCS mode does not use input signals configured to control ***fewer*** devices and ranks than are on the memory module; rather, it uses a certain number of input chip-select signals to control the ***actual number*** of devices and ranks on the module. That does not

satisfy the pertinent claim language, which is directed to the number of memory devices and ranks, not the number of chip-select signals.

For each of these independent reasons, Samsung is entitled to JMOL of noninfringement as to the '912 patent.

1. Netlist Failed To Prove That the Accused Products Are Reasonably Capable of Using the Allegedly Infringing Combination of Modes

Netlist relied on two optional modes to satisfy different elements of claim 16. Specifically, it relied on "PDA" mode for the "transmitted to only one DDR memory device at a time" limitation and "Encoded QuadCS" mode for the "input signals configured to control" limitation. *See* Tr. at 380:10-381:11, 403:11-404:3 (Mangione-Smith). These two modes do not satisfy those limitations for the reasons detailed below. Even if they did, however, that would not be sufficient to show infringement. As discussed further below, the transmission "to only one DDR memory device at a time" (only alleged to happen in PDA mode) must be in response to the particular "set of input signals" recited earlier in the claim (only alleged to be received in Encoded QuadCS mode). JX-2.45; *see infra* § III.A.2.b. Thus, to satisfy claim 16 as a whole under Netlist's infringement theory, the accused products would need to operate in both modes ***simultaneously***. Further—in view of the Court's conclusion that claim 16 is directed to "capability"—Netlist's theory required it to show that the accused products are "reasonably capable" of using "all of" the accused modes together. *See INVT*, 46 F.4th at 1374-80. Netlist failed to satisfy *INVT*'s reasonable capability standard in two respects.

First, *INVT* makes clear that when a claimed device "operates in an environment that involves the actions of another device" the other device's "operations must be known to determine whether the accused device infringes, i.e., is capable of performing the claimed functions." 46 F.4th at 1375. In *INVT*, for example, the claims at issue required receiving

signals with particular data encoding and modulation. *Id.* at 1366, 1374. The patentee alleged that the accused products were capable of receiving such signals from another device—a base station—but it failed to show "that a base station in fact ever sends the user device a data signal that is modulated and encoded" that particular way. *Id.* at 1371, 1377. The Federal Circuit thus held that the accused products did not satisfy the reasonable capability standard. *Id.* at 1380.

Claim 16 likewise "operates in an environment that involves the actions of another device"—a computer system. *See INVT*, 46 F.4th at 1375. It recites "receiving a set of input signals ***from the computer system***." JX-2.45. Thus, it is the computer system—and specifically the computer's memory controller—that determines what mode or modes the "input signals" are configured for. *E.g.*, Tr. at 361:22-362:9, 377:8-12 (Mangione-Smith) ("What determines what mode the module is operating in? A. So the host memory controller sends out information command signals that the RCD receives to put it in one operating more or another, whatever is appropriate."); *see also* Tr. at 342:22-24 (Jung) ("If a system controller does not activate PDA mode, then will PDA mode be used on a Samsung DDR4 product? A. No, it won't."). Thus, the operations of the computer system and its controller "must be known to determine whether the accused [products] infringe[]." *INVT*, 46 F.4th at 1375.

Just as the patentee in *INVT* offered no evidence of the base station's operation, *id.* at 1378-80, here, Netlist failed to offer any evidence of the computer system's operations. *See generally* Tr. at 366:8-413:8 (Mangione-Smith). Indeed, Dr. Mangione-Smith admitted he did not perform this analysis or even review any memory controller specifications or source code. Tr. at 501:14-508:10. Thus, Netlist has not established reasonable capability.

Second, *INVT* further requires "evidence or undisputed knowledge of an instance that the accused product performs the claimed functions when placed in operation." *Id.* at 1376. Netlist

did not identify such evidence. PDA and Encoded QuadCS modes are both individually optional, meaning that a customer could choose not to use either mode at all, let alone both modes simultaneously. *See* Tr. at 378:10-379:8 (Mangione-Smith) (acknowledging that Encoded QuadCS is but one of three possible modes that ***could*** be used), 519:19-521:7 (Mangione-Smith) (admitting that customers could decide not to use PDA mode). Indeed, the sum total of Dr. Mangione-Smith's testimony regarding using both modes together was the following:

> Q. Can those be used together?
> A. Sure.

Tr. at 404:7-8. He did not explain how both modes would be turned on together, in what context this purely hypothetical combination is purportedly possible, or identify any supporting evidence for this conclusion. *See generally* Tr. at 366:8-413:8 (Mangione-Smith). Such conclusory, *ipse dixit* testimony is not substantial evidence. *E.g.*, *MobileMedia*, 780 F.3d at 1172 ("Conclusory statements by an expert . . . are insufficient to sustain a jury's verdict."); *Kim v. ConAgra Foods, Inc.*, 465 F.3d 1312, 1320 (Fed. Cir. 2006) ("conclusory testimony" from an expert not sufficient to defeat JMOL).

Indeed, the Federal Circuit recently found even a significantly more extensive analysis insufficient to avoid JMOL of noninfringement in *Provisur Technologies, Inc. v. Weber, Inc.*, 119 F.4th 948, 952-55 (Fed. Cir. 2024). The accused products in *Provisur* were indisputably not sold in the accused "advance-to-fill" mode and there was no evidence that any customer ever operated them in this mode. *Id.* at 953. Nevertheless, the patentee provided an analysis—far more detailed than the one Dr. Mangione-Smith offered here—showing that the products were capable of being placed in "advanced-to-fill" mode. *See id.* at 953-55. Specifically, the patentee's expert identified a specific "human machine interface" which could modify the device's parameters to operate in "advance-to-fill" mode, identifying specific configuration

[redacted]

screens. *Id.* Nevertheless, the Federal Circuit held that this analysis was insufficient because (1) the configuration screens were available to only the defendant, not its end-user customers; and (2) the expert testified only that he "***could have***" reconfigured the accused products to meet the relevant limitation, not that he had actually been "able to configure it" that way. *Id.* at 954-55 (original emphasis).

Netlist's evidence here was even more deficient. Dr. Mangione-Smith did not identify any specific interface, "screens," or method that ***anyone***—let alone Samsung's customers—could use to simultaneously put Samsung's accused products in both PDA mode and Encoded QuadCS mode. Tr. at 366:8-413:8. He also did not testify that he ever actually placed any Samsung module into this combination of modes—only that the two modes hypothetically "[c]an . . . be used together" in an unspecified way under unspecified circumstances. Tr. at 404:7-8. Thus, his testimony is less adequate than the evidence found insufficient in *Provisur*.

Finally, Netlist adduced no evidence of Samsung—or anyone else—testing the simultaneous use of PDA mode and Encoded QuadCS mode in a memory module. Dr. Mangione-Smith opined that Samsung performs "validation testing" that would encompass testing of Encoded QuadCS mode. *See* Tr. at 383:5-385:8. However, he admitted that this testing was not performed on an accused memory module, but instead on only a particular component (the RCD) in isolation. *See id.* 384:2-6 (describing PX-2 as a "validation report on this particular RCD"), 384:19-25. Additionally, Dr. Mangione-Smith admitted that this testing is not performed using a computer system—as claim 16 requires, JX-2.45—but instead "using what's called an automated test equipment." Tr. at 383:9-384:6. Even more problematically, Dr. Mangione-Smith did not opine that this testing included simultaneous use of PDA mode; rather, he admitted that Encoded QuadCS mode was tested only "in combination with additional other

[redacted]

modes" such as "BC4 and BL8" that are not relevant to his infringement analysis. Tr. at 384:7-385:8. In short, Netlist provided no evidence that the accused combination of modes in question has ever been used or even tested.

Netlist utterly failed to introduce "evidence or undisputed knowledge of an instance that the accused product performs the claimed functions when placed in operation," as *INVT* requires. 46 F.4th at 1376. The Court, therefore, should grant JMOL of noninfringement.

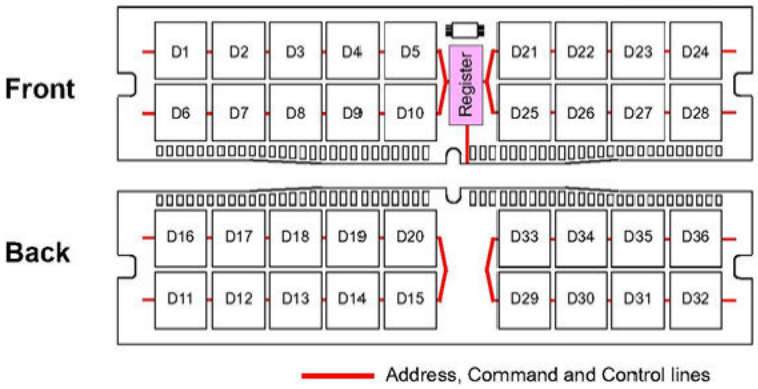
2. Netlist Failed To Show a Command Signal Transmitted to Only One DDR Memory Device at a Time in Response to a Row/Column Address Signal

Substantial evidence does not support the jury's finding that the accused products include a circuit receiving "a set of input signals comprising at least one row/column address signal" and "further responds to [that] set of input signals from the computer system by . . . transmitting the command signal . . . to only one DDR memory device at a time" for two independent reasons.

a. Commands Are Always Transmitted to Multiple Memory Devices in PDA Mode

At the outset, PDA mode does not satisfy the "wherein the command signal is transmitted to only one DDR memory device at a time" limitation. Dr. Mangione-Smith did not dispute that the accused products all have multiple DRAMs with "shared control address signals" which make up the "command code." Tr. at 375:22-376:1, 386:10-24, 404:18-405:3; JX-10.29; JX-28.9; JX-31.9. Nor could he, as the accused products' datasheets unambiguously show that every DRAM shares "Address, Command and Control lines" with the other DRAMs:

[redacted]



JX-28.12; *see also id.* at .13-14; JX-31.12-14. This structure, where "RCD outputs are connected to all the DRAMs," makes it "physically impossible" for only one DRAM to receive a "command . . . in PDA mode." Tr. at 342:25-343:3 (Jung).

Dr. Mangione-Smith did not opine otherwise. Although he testified that PDA mode allows "individual DRAMs" to be "***programmed*** one at a time" and that commands in PDA mode can be "sent" or "transmitted" "to a particular DRAM ***and executed***" individually, he pointedly never disputed that the commands are still transmitted to multiple DRAMs at the same time, even though only one DRAM ultimately executes the command. Tr. at 404:14-407:1. Claim 16 does not recite only one DRAM executing a command—it recites transmitting a command signal to only one memory device at a time. JX-2.45. [redacted] As a matter of common sense, a DRAM cannot "ignore" a command signal that was never transmitted to it.

Further, Dr. Mangione-Smith did not identify any plain meaning of "transmitted" that requires a device to actually execute the command. Tr. at 404:14-407:1. Nor could he as

[redacted]

"transmit" and "execute" are plainly not synonymous. Even where a term is not construed, an expert's testimony cannot support infringement unless "'a reasonable jury, given the record before it viewed as a whole, could have arrived at the conclusion it did.'" *Broadcom*, 543 F.3d at 696 (quoting *Dawn Equip. Co. v. Ky. Farms Inc.*, 140 F.3d 1009, 1014 (Fed. Cir. 1998)). Thus, the jury could not have reasonably concluded that PDA mode involves transmitting a command signal to only one memory device at a time.

b. PDA Mode Commands Cannot Be Transmitted in Response to a Row/Column Address Signal

Claim 16 requires (1) "receiving a set of input signals from the computer system . . . comprising at least one row/column address signal," (2) a circuit that "responds to a command signal and the set of input signals by . . . transmitting the command signal," and (3) that the "command signal is transmitted to only one DDR memory device at a time." JX-2.45. Even if Netlist had shown that PDA mode permits transmitting a command signal to only one memory device at a time, it did not show that this operation can be performed ***in response to a set of input signals comprising a row/column address signal***.

Dr. Mangione-Smith's infringement analysis regarding these limitations suffered from a fatal disconnect: he relied on PDA mode for the "transmitted to only one" limitation, yet relied on commands that cannot occur in PDA mode for the "row/column address signal" limitation. Specifically, Dr. Mangione-Smith testified that the only "example" of a capability to transmit a command signal to only one memory device in the accused products is PDA mode, Tr. at 403:11-404:3, [redacted]; *see also* Tr. at 514:15-519:5 (Mangione-Smith) (admitting that, for Samsung's products to infringe, they would need to have "an MRS command and a row/column address signal"); Tr. at 838:22-839:3 (McAlexander). The problem for Netlist is that the unrebutted

[redacted]

record shows that MRS commands ***never*** include row/column address signals. In analyzing the "row/column address signal" limitation, Dr. Mangione-Smith never identified a row/column address signal used with an MRS command. Instead, he opined only that the address input pins in Samsung's products "provide row address information and they provide column address information ***for read and write operations***"—operations that the modules cannot perform in PDA mode. Tr. at 366:8-371:9, 385:16-388:3.

Specifically, the unrebutted evidence shows that the only commands possible in PDA mode—MRS commands—cannot be sent in response to a row/column address signal. Not only was Mr. McAlexander's testimony on this point entirely unrebutted, Tr. at 835:23-840:9 (McAlexander), Samsung's SDRAM datasheet explicitly shows that a "Row Address" (RA) or "Column Address" (CA) signal is sent for only bank activate, read, and write commands—never for MRS commands. [redacted]

Ex. 1 at DDX11-40 (annotating JX-30.29).

Unable to dispute this simple fact, Netlist sought to confuse the issue by pointing to "address ***inputs***," generally, rather than to ***row/column*** address ***signals***, as claim 16 requires.

[redacted]

JX-2.45; Tr. at 874:25-875:4 (McAlexander); *see also* Tr. at 367:23-370:13 (Mangione-Smith). The evidence, however, is unequivocal that inputs A0 to A17 in the accused products are "address inputs," not row/column address signals. Tr. at 370:7-13 (Mangione-Smith) (admitting that "the As are indeed address ***inputs***"); [redacted][14]

Thus, the mere presence of address ***inputs*** does not satisfy the claim language.

Finally, the claim's plain language precludes any argument that the capability to receive a row/column address signal ***outside*** of PDA mode, such as in the context of read or write operations, is sufficient to satisfy claim 16. The clause "wherein ***the*** command signal is transmitted to only one DDR memory device at a time" refers to the same "command signal" (in red) that the claimed "circuit" must transmit in response to "***the*** set of input signals" (in blue), and "***the*** set of input signals" refers to the set recited earlier in the claim—which must include "at least one row/column address signal" (in green):

> 16. A memory module connectable to a computer system, the memory module comprising:
>
> . . .
>
> the circuit comprising a logic element and a register, the logic element receiving ***a set of input signals from the computer system***, ***the set of input signals*** comprising at least one row/column address signal, bank address signals, and at least one chip-select signal,
>
> ***the set of input signals*** configured to control a second number of DDR memory

[14] Mr. McAlexander explained, and Dr. Mangione-Smith never disputed, that the op-code is a "control signal" which is not a "row/column address signal," but rather "just the opposite." Tr. at 896:21-897:6.

[redacted]

> devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks . . . ,
>
> wherein the circuit further ***responds to a command signal*** and ***the set of input signals from the computer system*** by selecting one or two ranks of the first number of ranks and ***transmitting the command signal*** to at least one DDR memory device of the selected one or two ranks of the first number of ranks; and
>
> . . .
>
> ***wherein the command signal is transmitted to only one DDR memory device at a time***.

JX-2.45 (coloring added).

As a matter of both English grammar and established patent law, "[s]ubsequent use of the definite articles 'the' or 'said' in a claim refers back to the same term recited earlier in the claim." *E.g.*, *Wi-Lan, Inc. v. Apple, Inc.*, 811 F.3d 455, 462 (Fed. Cir. 2016); *see also Warner-Lambert Co. v. Apotex Corp.*, 316 F.3d 1348, 1356 (Fed. Cir. 2003) ("'It is a rule of law well established that the definite article "the" particularizes the subject which it precedes. It is a word of limitation as opposed to the indefinite or generalizing force of "a" or "an."'" (quoting *Am. Bus. Ass'n v. Slater*, 231 F.3d 1, 4-5 (D.C. Cir. 2000))). Thus, the command signal transmitted to only one device at a time must be sent in response to, among other things, a row/column address signal.

In sum, there is not a legally-sufficient evidentiary basis for a finding that the accused products respond to a set of input signals including a row/column address signal by transmitting a command signal to only one memory device at a time, as claim 16 requires. JX-2.45. The Court should grant JMOL of noninfringement.

[redacted]

3. Netlist Failed To Prove That the Accused Products Receive a Set of Input Signals Configured To Control Fewer Memory Devices and Ranks Than the Products Have

Claim 16 requires "a ***first number*** of DDR memory devices arranged in a ***first number*** of ranks" and "receiving a set of input signals from the computer system," where the set of input signals is "configured to control a ***second number*** of DDR memory devices arranged in a ***second number*** of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks." JX-2.45. The input signals that must be configured in this manner must include "at least one row/column address signal, bank address signals, and at least one chip-select signal." *Id.*

Netlist's infringement case (accusing Encoded QuadCS mode) dramatically oversimplified and mischaracterized these limitations. By the limitations' plain terms, they require both: (1) analyzing how the input signals are "configured," not how many input signals there are and (2) determining how many "DDR memory devices" the signals are configured to control, not just how many "ranks." *Id.* Netlist did not adduce evidence on any of these issues, instead focusing solely on comparing the number of input chip-select signals to output chip-select signals.[15] By focusing on the number of signals rather than the number of memory devices those signals are configured to control, as the claim recites, Netlist's evidence simply focused on the wrong part of the system.

The record uniformly shows that, in the accused products, the system is always "configured to control" the actual number of ranks and memory devices on the module, which is not the required "second number . . . ***less than the first number***" of devices and ranks, Samsung

[15] Netlist's closing even more egregiously conflated the number of input chip-select signals with the number of ranks, suggesting the claims are directed to a "smaller" and "larger set of chip select signals." Tr. at 1240:14-1241:5.

[redacted]

is entitled to JMOL of noninfringement.

a. Using Two Chip-Select Signals To Control Four Ranks Does Not Satisfy the Claim Language

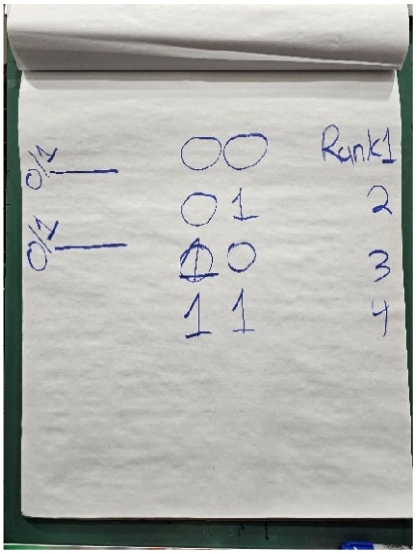
Claim 16 requires comparing the number of "memory devices" and "ranks" that the input signals are "configured to control" (i.e., the "second number") to the number of devices and ranks on the printed circuit board (the "first number" of devices and ranks). JX-2.45. Rather than applying this language, Dr. Mangione-Smith instead compared the ***number of chip-select signals*** input to the RCD to the number of chip-select signals output by the RCD. Tr. at 379:14-381:3 (Mangione-Smith) ("I've highlighted the second number of ranks in this case is equal to 2 ***because there are two chip-select inputs***. And the first number of ranks on the right-hand side I've highlighted in blue ***because there are four chip select outputs***. And two is less than four."). Claim 16 requires two different numbers of ranks of DRAM devices, not two different numbers of control signals; the comparison Dr. Mangione-Smith made simply is not the comparison the claim requires.

Critically, both experts agree that the input signals "determine which one of ***all the ranks on the DIMM*** will be active"—they are not configured to select among a smaller, "second number" of ranks. Tr. at 369:25-370:6 (Mangione-Smith); *see also* Tr. at 831:15-833:6, 893:15-894:25 (McAlexander) (explaining how two chip-select signals can be configured to control four ranks). Indeed, Dr. Mangione-Smith confirmed that the input chip-select signals "provide for ***external*** rank selection," meaning that "the ***host*** is able to determine which rank should be active or selected." Tr. at 369:13-370:6, 374:18-21.

Substantial evidence does not support the inference Netlist invited the jury to make—that the number of chip-select signals is a proxy for the number of ranks of memory devices the input signals are configured to control, as Netlist implied in closing. *E.g.*, Tr. at 1240:14-24. The

[redacted]

issue under the claim language is not whether chip-select signals control ranks, but ***how many*** ranks and memory devices they are "***configured*** to control." JX-2.45. The undisputed evidence shows that the two input chip-select signals in Encoded QuadCS mode are "configured" to control four ranks, not two. Tr. at 369:13-370:6, 374:18-21 (Mangione-Smith), 831:15-833:6, 893:15-894:25 (McAlexander) (explaining how two "encoded" signals correspond to four unique outputs and thus are configured to control four ranks). Samsung illustrated this concept at trial with a graphic (below),[16] which shows how Encoded QuadCS mode uses two input signals (shown on the left) to control four ranks (shown on the right):



Netlist did not dispute the accuracy of this graphic or Mr. McAlexander's explanation of input signal encoding.

The datasheets confirm these facts. [redacted]

[redacted]

[16] The third row of the middle of the graphic should reflect the combination of "10." Tr. at 894:19-22 (McAlexander). Thus two signals, each of which can be set to "0" or "1" corresponds to four unique combinations, each of which correspond to a particular rank: 00, 01, 10, or 11. *Id.*; *see also id.* 379:18-380:1 (Mangione-Smith) (admitting chip select signals in Encoded QuadCS Mode are "encoded so you can cover more range with them").

[redacted] Thus, unlike the claimed invention, where a "circuit" ***on the memory module*** "selects one or two ranks," JX-2.45, in the accused products, the determination of "which one of all the ranks on the DIMM" to activate is made "external to the RCD" (the alleged "circuit") by input signals coming from the host memory controller configured to control all the ranks. Tr. at 369:13-370:6 (Mangione-Smith); *see also* Tr. at 366:3-5 (Mangione-Smith). Further, a technical specification for all Samsung's DDR4 memory modules indicates that the module communicates the correct number of ranks and memory devices on the module to the memory controller. DTX-28.1; DTX-28.20. The controller then uses this data to configure its signals to correspond to the actual numbers of ranks and memory devices present on the module. Tr. at 830:13-23 (McAlexander).

Because all the evidence addressing the pertinent issue under the claim language shows that the input signals in Encoded QuadCS mode are configured to control ***all*** the memory devices and ranks on the module, they are not "configured to control a second number of DDR memory devices arranged in a second number of ranks" ***less than*** the respective first number of memory devices and ranks. JX-2.45. Therefore, no reasonable jury could have found that the accused products satisfy these limitations.

b. Netlist Failed To Address How Many Memory Devices the Accused Input Signals Are "Configured To Control"

Finally, claim 16 separately requires both that (1) "the second number of DDR memory devices [is] smaller than the first number of DDR memory devices ***and***" (2) "the second number of ranks [is] less than the first number of ranks." JX-2.45. Dr. Mangione-Smith never identified,

[redacted]

let alone compared, the alleged "first" and "second" number of ***memory devices*** in any accused mode of any accused product—he purported to address only the numbers of ranks. Tr. at 379:14-381:11.

There is no evidentiary basis to conclude that input signals "configured to control" fewer ranks would also be "configured to control" fewer memory devices, and any such argument is "unsupported speculation" which is "insufficient to support the jury's verdict as a matter of law." *Genmoora Corp. v. Moore Bus. Forms, Inc.*, 939 F.2d 1149, 1163 (5th Cir. 1991). Indeed, the memory module could have the same number of ranks that the input signals are configured to control but more memory devices by using memory devices with a lower bit-width than the computer system expects, as the '912 patent explicitly contemplates. *E.g.*, JX-2.24 (4:42-58), .26 (8:59-64), .28 (11:5-42) ("In an exemplary embodiment, two 512-Mb memory devices, each with a 128 M×4-bit configuration, are used to simulate one 1-Gb memory device having a 128 M×8-bit configuration."). Conversely, the memory module could have more ranks and the same number of devices by using a higher bit-width per device. *See id.*

The unrebutted evidence establishes that the accused products each contain a serial presence detect (SPD) device which provides the computer's memory controller with "the number of devices," and the controller "configure[s] its signals to correspond to the actual number" of "devices that are on the memory module," including in Encoded QuadCS mode. Tr. at 829:18-831:1, 832:10-833:6 (McAlexander); DTX-28.5 ("The system BIOS will acquire information . . . to properly configure the system's memory controller"); DTX-28.20. Because there is no factual dispute that the set of input signals are configured by the computer system's memory controller based on the accurate number of memory devices shown in the SPD, there is no non-speculative basis for the jury to have found that the input signals are "configured to

[redacted]

control" a smaller number of memory devices. Thus, JMOL is appropriate. *Genmoora*, 939 F.2d at 1163.

B. There Is No Evidentiary Basis To Conclude That the '912 Patent's Written Description Adequately Discloses Input Signals "Configured To Control" Fewer Memory Devices and Ranks Than the Module Has

The Court should enter JMOL of invalidity for the '912 patent because the specification lacks written description support for claim 16 as Netlist applied it in this case. Claim 16 requires "receiving a set of input signals from the computer system," that is "configured to control" fewer memory devices and ranks than are on the memory module. JX-2.45; *see also supra* § III.A.3. As explained above, Netlist ignored this limitation at trial and asked the jury to focus on irrelevant issues, such as the fact that the number of chip-select signals input in the accused Encoded QuadCS mode is less than chip-select signals outputs. *Supra* § III.A.3.a; *see also* Tr. at 380:21-381:3 (Mangione-Smith). Netlist focused on this distraction because, in the accused products, the memory module informs the memory controller of the ***actual*** number of ranks and devices on its module, and the memory controller can directly control and address those ranks and devices. Tr. at 379:18-380:1 (Mangione-Smith) (admitting that in Encoded QuadCS Mode "the two chip select signals we say they're encoded ***so you can cover more range with them***"); Tr. at 831:15-833:6, 893:15-894:25 (McAlexander). Under Netlist's broad interpretation of claim 16 as covering this arrangement (which the jury necessarily applied to find infringement), the claim lacks written description support and is invalid. *See Rivera*, 857 F.3d at 1321.

Unlike the accused products, where the computer's memory controller knows how many ranks and memory devices are on the module and configures its signals accordingly, the '912 patent uniformly teaches that the input signals are "configured to control" ***fewer*** ranks and devices because the computer sending the signals believes there are fewer ranks and devices on the module than there actually are. For example, the patent teaches that the module's SPD,

which ordinarily provides accurate information about the module to the computer's memory controller, should instead "characterize the memory module 10 as having fewer ranks of memory devices than the memory module 10 actually has." JX-2.27 (10:31-44); *see also id.* (9:24-37) (describing how SPDs normally work). Thus, "even though the memory module 10 actually has the first number of ranks of memory devices 30, the memory module 10 simulates a virtual memory module by operating as having the second number of ranks of memory devices 30." JX-2.27 (7:9-19). As a result, in the disclosed invention, the memory controller does not know the ***actual*** number of memory devices and ranks on the memory module and sends input signals "configured to control" ***fewer*** devices and ranks. *See* Tr. at 821:16-831:1 (McAlexander).

Although this disclosure constitutes an example of input signals "configured to control" fewer ranks and devices than the module has, it is not adequate written description support under Netlist's interpretation of claim 16 which was much broader. Rather, for the '912 patent to be valid, its written description must "sufficiently demonstrate[] that the inventors possessed the ***full scope*** of the claimed invention." *Juno*, 10 F.4th at 1336 (Fed. Cir. 2021); *see also Cooper Cameron Corp. v. Kvaerner Oilfield Prods., Inc.*, 291 F.3d 1317, 1323 (Fed. Cir. 2002) ("[A] broad claim is invalid when the entirety of the specification clearly indicates that the invention is of a much narrower scope."). The '912 patent is therefore invalid unless its written description is commensurate in scope with what the claims cover.

There is no dispute that, unlike the invention described in the '912 patent, the SPD in Samsung's products accurately informs the memory controller about the number of memory devices and ranks on the module. *E.g.*, Tr. at 825:1-831:1 (McAlexander); *see also* DTX-28.1, .5, .20, .23. As a result, a memory controller knows exactly how many ranks and devices it is

[redacted]

controlling on a Samsung memory module. Tr. at 821:16-831:1 (McAlexander).[17] Mr. McAlexander explained, without rebuttal (because Netlist failed to present a rebuttal case defending the patent's validity), that the '912 patent contains no written description support for such a configuration, Tr. at 840:10-22, rendering claim 16 invalid under Netlist's interpretation. *See Atl. Rsch.*, 659 F.3d at 1355. Accordingly, the Court should enter JMOL that the '912 patent is invalid. *ParkerVision*, 621 F. App'x at 1023 (noting "no basis on which a reasonable jury could reject" the expert's "uncontradicted testimony").

IV. The Court Should Enter Judgment as a Matter of Law of Noninfringement and Invalidity of the '417 Patent

A. Netlist Failed To Offer Substantial Evidence That the Accused Products Satisfy the "Data Buffer Control Signals" Limitation

Substantial evidence does not support the infringement verdict because Netlist failed to prove that the accused DDR4 LRDIMM products infringe the "data buffer control signals" limitations under their plain meaning. The asserted claims require multiple "data buffer control signals" (as indicated by the plural "signal**s**") that must (1) be output by "logic" in response to a single read or write memory command and (2) cause "circuitry" to transfer data. JX-1.59 (cl. 1). Netlist failed to adduce any evidence (much less substantial evidence) that the accused products satisfy each of these requirements.

At trial, Netlist disregarded the plain and ordinary meaning of "buffer control signal**s**" by arguing that a ***single*** signal called "BCOM" satisfies this term. Tr. at 469:8-11. As explained below, the undisputed evidence shows that the BCOM signal is a single encoded signal made up of four bits. [redacted] 331:6-25, 424:17-21, 438:25-439:4, 546:7-549:10, 550:21-551:3, 844:2-6. Thus, Netlist's infringement theory rests on equating each bit as a

[17] [redacted]

[redacted]

separate "buffer control signal"—a theory that goes well beyond the term's plain meaning. Indeed, there is no evidentiary basis for equating bits and control signals. The claim language instructs otherwise and confirms that a ***single*** signal may have multiple bits by describing signals as "N-bit wide." JX-1.59 (cl. 1). For example, claim 1 recites a memory bus including "data signal lines," where each line is a data signal line, and later refers to the signal lines collectively as being "N-bit wide." *Id.*; *see also* JX-1.49 (22:66) (referencing a "address signal bit"); JX-1.50 (23:3) (same); JX-1.50 (23:42) (referring to a "[n]umber of row address bits").

The BCOM signal is one buffer control signal, not four. The parties' experts agree on this point. Netlist's technical expert, Dr. Mangione-Smith, repeatedly testified that BCOM is a single signal. Tr. at 424:17-21, 438:25-439:4, 546:7-549:10, 550:21-551:3. Samsung's technical expert, Mr. McAlexander, further testified that BCOM is one "four-bit encoded signal." *Id.* at 844:2-6. Mr. Davey, the engineer who designed the RCD component that generates the BCOM signal, consistently testified that BCOM is a single control signal. Tr. at [redacted] 331:6-25. He also explained that the BCOM signal is a single, four-bit signal: [redacted] Tr. at 331:6-7.

This testimony is consistent with the documentation. For example, the data sheet for the RCD component shows one BCOM signal (highlighted in yellow) as an output.

[redacted]

[redacted]

[redacted]

[redacted]

[redacted]

[redacted]

Other claim language further demonstrates why Netlist cannot conflate individual bits with "buffer control signals" without disregarding the claim's plain meaning. The claims do not simply require multiple signals. They require multiple "data buffer ***control*** signals" that must be

[redacted]

output in response to a memory command ***and*** that those multiple "data buffer control signals" cause the circuitry to transfer data. JX-1.59 (cl. 1). The evidence shows, however, that the BCOM signal operates as a single control signal for data transfer. [redacted]

Second, Mr. Davey offered unrebutted testimony that all four bits of the BCOM signal must be set properly to control the buffer:

[redacted]

Tr. at 331:18-25. Mr. McAlexander similarly explained that BCOM must include "all four bits in order to decode it to determine what it says." Tr. at 845:8-12.

Netlist's assertion that a single four-bit encoded signal constitutes multiple "buffer control signals" ignores the word "control" in "buffer ***control*** signals." [redacted] Whether each bit could be a signal is not the pertinent question, however. The question for infringement is whether each bit is a separate "buffer control signal," and Netlist provided no evidence on this point. To the contrary, the evidence uniformly shows that the accused products require all four bits of the BCOM signal to control the buffer. [redacted] JX-11.18; JX-12.39; JX-14.23.

Finally, Netlist ignored the claim language surrounding the "buffer control signals." For the claim requirement that the logic outputs multiple data buffer control signals ***in response to a***

[redacted]

memory command, JX-1.59 (42:54-62), Dr. Mangione-Smith did not identify any "memory command" that causes BCOM to be outputted or show that the accused "logic" (i.e., the RCD) outputs the BCOM signal in response to a memory command. Tr. at 468:21-471:5. Netlist similarly offered no evidence that the alleged "circuitry" in the accused products (i.e., the data buffers) is "configurable to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks ***in response to the [multiple] data buffer control signals***." JX-1.59 (42:54-62). Dr. Mangione-Smith did not even mention this limitation,[18] let alone prove that one or multiple bits of the BCOM signal are used to transfer a burst of N-bit wide data signals between the memory bus and the memory devices in the accused products.

For these reasons, the record lacks substantial evidence that the accused DDR4 LRDIMM products infringe any asserted claim of the '417 patent.

B. There Is No Evidentiary Basis To Conclude That the '417 Patent's Written Description Adequately Discloses Distributed Data Buffers

The Court should enter JMOL of invalidity for the '417 patent because the specification lacks written description support for the claims as Netlist applied them in this case. Here, Netlist broadened the scope of the invention beyond the specification's teaching in an attempt to ensnare the accused products, which use multiple distributed data buffers as opposed to the single buffer disclosed in the '417 patent. Netlist's impermissible broadening invalidates the patent. *See Rivera*, 857 F.3d at 1321.

[18] Dr. Mangione-Smith testified that data signals must be transferred in accordance with CAS latency, but he did not say that this transfer is done "in response to the data buffer control signals." *See* Tr. at 474:15-476:14 (discussing data transfers through the buffer's data paths—no buffer control signals), 476:15-482:3 (CAS latency discussion—no buffer control signals), 482:4-482:7 (overall conclusion and final discussion of claim 1). As a result, the record is devoid of any evidence from which any jury reasonably could have found that the accused products meet this limitation.

[redacted]

The claims recite "circuity" for transferring N-bit wide data signals: "***circuitry*** coupled between the data signal lines in the N-bit wide memory bus and corresponding data pins of memory devices in each of the plurality of N-bit wide ranks, the circuitry being configurable ***to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks*** in response to the data buffer control signals and in accordance with an overall CAS latency of the memory module." JX-1.59 (cl. 1). Netlist alleged the collection of distributed data buffers in Samsung's DDR4 LRDIMM products—consisting of at least nine separate buffers—satisfied the claimed "circuitry." Tr. at 473:18-473:25 (Mangione-Smith); JX-36.10; JX-36.11; JX-36.12.[19]

The evidence demonstrates that the '417 patent does not provide written description support for broad claims covering a memory module with distributed data buffers, let alone one where the distributed data buffers "transfer the burst of N-bit wide data signals." JX-1.59. To the contrary, the '417 patent refers to its proposed "circuitry" in the singular as a single "circuit 40." *E.g.*, JX-1.42 (7:4-9, 7:17-39, 7:61-8:9, 8:10-61); JX-1.43 (9:7-46). Every embodiment in the patent teaches using a single data buffer, *id.*, and the accompanying figures show only a single circuit representing "circuit 40," not multiple buffers as found in the accused products. JX-1.16 (Fig. 1); JX-1.18 (Figs. 3A, 3B); JX-1.19 (Figs. 4A, 4B); JX-1.20 (Figs. 5A, 5B); JX-1.21 (Figs. 5C, 5D); JX-1.24 (Figs. 8A, 8B); JX-1.25 (Figs. 8C, 8D); JX-1.26 (Fig. 9A); JX-1.27 (Fig. 9B); JX-1.29 (Figs. 10A, 10B); JX-1.30 (Figs. 11A, 11B). Mr. McAlexander similarly testified that he did not see any description in the '417 patent about distributed buffers. Tr. at

[19] Netlist accused the collection of data buffers as the claimed "circuitry" because each data buffer is only eight-bits wide, but the claims require that the circuitry "transfer [a] burst of N-bit wide data signals," and Netlist's expert asserted that the number represented by "N" must be 72, not eight. JX-1.59; Tr. at 335:7-14 (Mangione-Smith).

[redacted]

846:12-847:4.

The '417 patent's failure to disclose a memory module with distributed data buffers is not surprising in light of the named inventor's candid testimony that he did not invent distributed data buffers—the very same buffers that Netlist alleged are claimed. In fact, Mr. Jeffrey Solomon ***never worked on distributed buffers*** during his time at Netlist, and said he was "not even sure what – what data buffer means in this context [of the '417 patent]." Tr. at 785:18-786:12.

Given this admission, no reasonable jury could have found that the named inventor actually had possession of claims covering distributed buffers, as required to satisfy the written description requirement. *See Ariad*, 598 F.3d at 1351 ("[T]he specification must describe an invention understandable to that skilled artisan and show that the inventor actually invented the invention claimed."); *Vas-Cath Inc. v. Gambro, Inc.*, 935 F.2d 1555, 1562-63 (Fed. Cir. 1991) (examining "whether the disclosure of the application relied upon reasonably conveys to the artisan that the inventor had possession at that time of the later claimed subject matter" (internal quotation, citation omitted)); *see also Nuvo Pharms. (Ireland) Designated Activity Co. v. Dr. Reddy's Lab'ys. Inc.*, 923 F.3d 1368, 1381 (Fed. Cir. 2019) ("Although inventor testimony cannot establish written description support where none exists in the four corners of the specification, it illuminates the absence of critical description in this case.").

Notably, Netlist failed to present a rebuttal case for the '417 patent's invalidity. Dr. Mangione-Smith identified nothing in the specification disclosing using distributed buffers to transfer less than the entire N-bits of the rank. Consequently, the record lacks any evidence showing the specification supports claims broad enough to cover anything but a single data buffer. *ParkerVision*, 621 F. App'x at 1023 (noting "no basis on which a reasonable jury could

[redacted]

reject" the expert's "uncontradicted testimony").

Accordingly, the Court should enter JMOL that the '417 patent is invalid.

V. The Court Should Enter Judgment as a Matter of Law of No Willful Infringement

Netlist failed to introduce evidence that Samsung had knowledge of the asserted patents and engaged in "deliberate or intentional infringement" with a "specific intent to infringe at the time of the challenged conduct," as required for a claim of willful infringement. *Provisur*, 119 F.4th at 955-56 (reversing denial of JMOL of no willfulness, where the defendant knew of the asserted patents but "there [was] no evidence [the defendant] knew of its alleged infringement"); *SRI Int'l*, 14 F.4th at 1330 ("[T]he concept of 'willfulness' requires a jury to find no more than deliberate or intentional infringement." (quotation, citation omitted)); *Baxter Healthcare LLC v. Baxalta Inc.*, 989 F.3d 964, 988 (Fed. Cir. 2021) (affirming grant of JMOL of no willfulness). Samsung is therefore entitled to JMOL of no willful infringement.

A. Netlist Failed To Provide Substantial Evidence of Deliberate or Intentional Infringement

The Court ruled that Samsung did not infringe (and thus could not willfully infringe) before Netlist's purported termination of the JDLA on July 15, 2020. *See* Dkt. 727 at 27; Tr. at 135:20-24 (jury instructions). Netlist thus had to prove that Samsung's conduct after July 15, 2020 rose to the level of deliberate or intentional infringement. But Netlist offered no evidence that Samsung took any actions, with respect to ***any*** asserted patent, after July 2020 or the filing of this action—beyond simply continuing to sell the accused products. Netlist rested instead on vague documents from before the JDLA's alleged termination, none of which show that Samsung had reason to investigate Netlist's patents, let alone that Samsung actually formed a belief that the patents were infringed. Nor could they, as Samsung was indisputably licensed to Netlist's patents prior to the JLDA's alleged termination in July 2020. Thus, no reasonable jury

[redacted]

could have found willfulness on this record.

1. Documents from Before July 2020 Do Not Show Willful Infringement

Even setting aside the fact that Samsung was licensed to Netlist's patents prior to July 2020, the documents Netlist relies on prior to July 2020 do not support a finding of willfulness. In particular, Netlist attempted to prove willfulness by arguing that Samsung had knowledge of Netlist's technology through a HyperCloud presentation Netlist gave to Texas Instruments (PX-26) and a subsequent Texas Instruments ("TI") presentation at JEDEC. Tr. at 302:13-24 (Milton); 304:17-24 (Milton); 983:4-984:9 (Halbert). Netlist failed, however, to provide any evidence that its presentation to TI (PX-26) was ever given to Samsung or that TI's subsequent presentation at JEDEC incorporated any of Netlist's technology or ideas. Tr. at 985:1-5 (Halbert). Regarding Netlist's HyperCloud presentation to Samsung in 2012 (PX-12, PX-13), this presentation did not identify the asserted patents or allege that Samsung infringed the asserted claims. In fact, the '417 and '608 patents and the '912 patent's reexamination certificate had not even issued in 2012. JX-1.2, JX-2.43, JX-3.2.

In contrast, Samsung presented unrebutted testimony that DDX3-5, a patent list Netlist sent to Samsung in November 2016, did not list ***any of the asserted patents*** even though Netlist said the identified patents "cover" the products accused of infringement in this case—DDR4 LRDIMM and DDR4 RDIMM. Tr. at 764:12-765:10 (Ji); Ex. 1 at DDX3-5. Indeed, this communication informing Samsung that the '912 patent does not "cover" DDR4 LRDIMM and RDIMM products (by virtue of its absence from the list) was the last communication Netlist made about the '912 patent before it purported to terminate the JDLA, precluding any inference that Samsung knew the accused products infringed when its license (allegedly) terminated.

The '912 patent. For the '912 patent, Netlist also relied on an April 2015 Netlist presentation (PX-30) to establish willful infringement. However, Mr. Ji testified that, when

[redacted]

Netlist presented PX-30 to Samsung, "Netlist did not mention any individual patents," and did not suggest that Samsung infringed any of the patents listed in PX-30. Tr. at 757:4-24. Mr. Milton was not at the April 2015 meeting, Tr. at 283:22-284:4, and thus the jury could not have reasonably relied on his speculation about what happened at this meeting. Further, the '912 patent was undergoing re-examination and had not issued in its current form in April 2015. JX-2.43 (dates of reexamination); JX-2.45 (showing amendments to claim 16 in italics). These facts foreclose any inference that PX-30 led to Samsung's believing the accused products infringe.

Netlist further relied on a patent disclosure it made to JEDEC (JX-46), but this disclosure was directed to the ***DDR3*** JEDEC standard, not DDR4. Tr. at 981:2-17 (Halbert). The disclosure also does not contain any charge of infringement by Samsung or even the JEDEC standard. JX-46. Indeed, Netlist admitted that the '912 patent is not essential to the DDR4 standards. Tr. at 267:16-18 (Milton). As a result, no reasonable jury could have found that JX-46 evidences intentional infringement by Samsung.

The '417 and '608 patents. To prove willful infringement of the '417 patent, Netlist relied again on Netlist's April 2015 presentation (PX-30), which mentions patents genealogically related to the '417 patent. Tr. at 250:18-251:25 (Milton). PX-30 does not mention the '417 patent, ***which had not even issued at the time***. Knowledge of one patent in a family does not establish knowledge of a related patent. *See Intell. Ventures II LLC v. Sprint Spectrum, L.P.*, No. 2:17-CV-00662-JRG-RSP, 2019 WL 1987172, at *2 (E.D. Tex. Apr. 12, 2019) ("[K]nowledge of other patents in the same portfolios, with some of those being within the same family as the asserted patents, [is] insufficient to defeat a motion for summary judgment for pre-suit willfulness."), *adopted by* 2019 WL 1979866 (E.D. Tex. May 2, 2019). PX-30 also does not include any charge of infringement.

[redacted]

Netlist further relied on its patent disclosures to JEDEC (JX-48 and JX-49), but these disclosures mention only patents related to the '417 and '608 patents, not the asserted patents themselves and, like PX-30, they do not include any charge of infringement. Netlist's reliance on the October 2020 letter Netlist's counsel sent to Samsung, Ex. 2 at PD2.129 (citing IX-162), fails for the same reason—the letter lists only patents genealogically related to the '417 and '608 patents. Tr. at 253:20-255:8 (Milton); Tr. at 927:16-928:2 (Yoon). Notably, the letter omits the '608 patent even though it had already issued by October 2020. JX-3.2.

2. Unrebutted Evidence Shows No Willfulness

Netlist presented no evidence that it told Samsung it was infringing the asserted patents before filing suit. Chuck Hong, Netlist's CEO, confirmed that Netlist did not inform Samsung of any alleged infringement—for any asserted patent—***before*** Netlist purported to terminate the JDLA. Tr. at 1034:17-1035:3; 1036:12-15; *see also* Tr. at 757:21-24, 765:14-17 (Ji). The record likewise contains no evidence that Netlist informed Samsung of the alleged infringement ***after*** the purported license termination until Netlist filed suit. As Mr. Junseon Yoon testified, Netlist never told Samsung that Netlist thought the Samsung accused products infringe before filing its complaints. Tr. at 926:13-929:1, 934:18-936:17. He explained, for example, that the October 2020 letter mentioned that Samsung might be using some Netlist patents ***other than the patents-in-suit*** and did not allege that Samsung infringed the asserted patents. Tr. at 927:16-928:2. Mr. Yoon also testified that the June 2022 letter similarly did not allege that Samsung infringed any of the asserted patents. Tr. at 936:1-17. Notably, Netlist did not enter the June 2022 letter into evidence, making Mr. Yoon's testimony the only evidence on this issue.

Post-suit, Netlist failed to show any conduct by Samsung beyond continuing to sell the accused products—which is legally insufficient to demonstrate willfulness. *See Gustafson Inc. v. Intersystems Indus. Prods., Inc.*, 897 F.2d 508, 511 (Fed. Cir. 1990) (There is no "universal rule

[redacted]

that to avoid willfulness one must cease manufacture of a product immediately upon learning of a patent, or upon receipt of a patentee's charge of infringement, or upon the filing of suit."); *HOYA Corp. v. Alcon Inc.*, 713 F. Supp. 3d 291, 318 (N.D. Tex. 2024) (granting summary judgment of no willful infringement because "the record indicates that, at most, Alcon has continued to sell the accused UltraSert product after the Complaint was filed in December 2020 and Alcon became aware of HOYA's infringement claims. Such conduct, without more, is insufficient to create a fact question as to willfulness, particularly given that the UltraSert was first released in 2015, years before suit."). Netlist also failed to rebut Samsung's evidence that it has maintained a good faith belief that it does not infringe the asserted patents, and that the asserted patents are invalid. Such good-faith reliance on reasonable defenses bars a willfulness finding. *See id*.

Specifically, Mr. Yoon testified that Samsung conducted an investigation and concluded that Samsung did not infringe. Tr. at 929:2-930:1, 932:20-22 ('912 patent); 937:2-9 ('417 and '608 patents). His investigation showed that "engineers were not aware of any of Netlist's patents at the time of their development of the accused products." Tr. at 939:10-14. Mr. Yoon also testified that, based on a separate investigation, Samsung concluded they patents are invalid. Tr. at 933:8-11, 934:6-14 ('912 patent); 937:2-9 ('417 and '608 patents). Netlist's argument that Mr. Yoon's investigation relied on only Mr. Seung-Mo Jung, who "testified that he [himself] did nothing to investigate who used [Netlist's] patents," was insufficient to rebut Mr. Yoon's testimony that he was part of a "very thorough investigation" that involved "dozens of patent analysts" and engineers. Tr. at 929:2-15; 932:14-19.[20]

[20] Contradicting Mr. Yoon's undisputed testimony, Netlist argued in closing that Samsung employees failed to investigate infringement. Tr. at 1237:3-13. However, even assuming that

[redacted]

Finally, Netlist never identified any Samsung employee with knowledge of the asserted patents and alleged infringement who decided to continue selling the accused products—let alone anyone with sufficient authority such that his acts and knowledge can be imputed to Samsung. *See Staub v. Proctor Hosp.*, 562 U.S. 411, 418 (2011) ("[T]he malicious mental state of one agent cannot generally be combined with the harmful action of another agent to hold the principal liable for a tort that requires both."); *Potter Voice Techs., LLC v. Apple Inc.*, 24 F. Supp. 3d 882, 886 (N.D. Cal. 2014) ("In the context of willful infringement, it is safe to say that the employees required to have knowledge of the asserted patent must have some connection to the decision willfully to infringe.").

B. No Reasonable Jury Could Have Found That Samsung Was Willfully Blind

The Court instructed the jury, over Samsung's objection, that it could substitute the willful blindness standard for the "deliberate or intentional" standard required for a finding of willful infringement. Tr. at 1187:6-22, 1220:13-21. Although willful blindness can support an inducement claim under § 271(b), *see Global-Tech Appliances, Inc. v. SEB S.A.*, 563 U.S. 754, 765–66 (2011), neither the Supreme Court nor the Federal Circuit has recognized this theory for a claim of willful infringement. Further, *Global-Tech* held only that willful blindness could substitute for a showing of actual knowledge of a patent, not that it could satisfy the *mens rea* requirement, as the Court's instruction permitted here. *See Ansell Healthcare Prods. LLC v. Reckitt Benckiser LLC*, No. 15-CV-915-RGA, 2018 WL 620968, at *7 (D. Del. Jan. 30, 2018) ("[I]nsofar as willful blindness does apply in willful infringement cases, it only substitutes for

---

Netlist's argument was true, a failure to investigate "is unquestionably insufficient to support a finding of willfulness." *Huawei Techs. Co. v. T-Mobile US, Inc.*, No. 2:16-CV-00052-JRG-RSP, 2017 WL 11638984, at *5 (E.D. Tex. Sept. 29, 2017); *see also SRI Int'l, Inc. v. Cisco Sys., Inc.*, 930 F.3d 1295, 1309 (Fed. Cir. 2019) (engineers' failure to read patents did not support a willfulness finding). Such attorney argument is legally insufficient to support jury verdict. *See Intell. Ventures I*, 870 F.3d at 1331.

actual knowledge, as opposed to egregious behavior.").

Even if willful blindness were a viable theory, Samsung would be entitled to JMOL. Willful blindness requires that "(1) [t]he defendant must subjectively believe that there is a high probability that a fact exists and (2) the defendant must take deliberate actions to avoid learning of that fact." *Global-Tech*, 563 U.S. at 769; *contra* Tr. at 1220:17-21 (jury instruction incorrectly allowing willful blindness to be found through mere indifference to another's rights). As discussed, there was no evidence that Netlist informed Samsung of the alleged infringement until filing suit, and none of the communications from before or during the license period are sufficient to show that anyone at Samsung believed, years later, that infringement was highly likely and took deliberate steps to avoid this knowledge—let alone that any such individual had responsibility for the alleged infringement. *See Staub*, 562 U.S. at 418. Evidence that Samsung did not investigate possible infringement of Netlist patents as they issued (or emerged from reexamination) is insufficient to show that Samsung took "***active efforts*** . . . to avoid knowing about the infringing nature" of the accused products, *Global-Tech*, 563 U.S. at 770, particularly where Netlist's last communication about the Netlist patents that allegedly "cover" DDR4 LRDIMM and RDIMM did not list any of the patents-in-suit, PX-30, and Netlist did not include the '417 or '608 patents in its initial complaint, Tr. at 934:18-935:25, 936:18-937:4 (Yoon), thus showing that even Netlist did not know of the alleged infringement before it filed suit.

CONCLUSION

For the foregoing reasons, the Court should enter judgment of noninfringement, invalidity, and no willfulness in favor of Samsung.

[redacted]

Dated: December 30, 2024

Respectfully submitted,

By: */s/ Ruffin B. Cordell*

Melissa Richards Smith
melissa@gillamsmith.com
GILLAM & SMITH, LLP
303 South Washington Ave.
Marshall, Texas 75670
Telephone: (903) 934-8450
Facsimile: (903) 934-9257

J. Travis Underwood
Texas Bar No. 24102587
travis@gillamsmithlaw.com
GILLAM & SMITH, LLP
102 North College Avenue, Suite 800
Tyler, Texas 75702
Telephone: (903) 934-8450
Facsimile: (903) 934-9257

Brian R. Nester
DC Bar No. 460225
bnester@cov.com
COVINGTON & BURLING LLP
One CityCenter 850 Tenth Street, N
Washington, DC 20001-4956
Telephone: (202)-662-6000

Alice J. Ahn
CA Bar No. 271399/DC Bar No. 1004350
aahn@cov.com
COVINGTON & BURLING LLP
415 Mission Street, Suite 5400
San Francisco, CA 94105
Telephone: (415) 591-7091
Facsimile: (415) 955-6571

Ruffin B. Cordell
TX Bar No. 04820550
cordell@fr.com
Michael J. McKeon
D.C. Bar No. 459780
mckeon@fr.com
Lauren A. Degnan
D.C. Bar No. 452421
degnan@fr.com
Daniel A. Tishman
DC Bar No. 1013923
tishman@fr.com
FISH & RICHARDSON P.C.
1000 Maine Avenue, SW
Washington, DC 20024
Telephone: (202) 783-5070
Facsimile: (202) 783-2331

Francis J. Albert
CA Bar No. 247741
albert@fr.com
FISH & RICHARDSON P.C.
12860 El Camino Real, Ste. 400
San Diego, CA 92130
Telephone: (858) 678-5070
Facsimile: (858) 678-5099

Thomas H. Reger II
reger@fr.com
Texas Bar No. 24032992
FISH & RICHARDSON P.C.
1717 Main Street, Suite 5000
Dallas, Texas 75201
Telephone: (214) 747-5070
Facsimile: (214) 747-2091

Attorneys for Defendants Samsung Electronics Co., Ltd.; Samsung Electronics America, Inc.; and Samsung Semiconductor, Inc.

[redacted]

CERTIFICATE OF SERVICE

I hereby certify that a true and correct copy of the foregoing document was filed electronically in compliance with Local Rule CV-5 on December 30, 2024. As of this date, all counsel of record have consented to electronic service and are being served with a copy of this document through the Court's CM/ECF system under Local Rule CV-5(a)(3)(A) and via electronic mail.

/s/ Ruffin B. Cordell

[redacted]